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Investigation of CdS Nanowires and Planar Films for Enhanced Performance as Window Layers in CdS-CdTe Solar Cell Devices

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Dr. Vijay Singh, Major Professor

Dr. Zhi David Chen, Director of Graduate Studies

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THESIS

A thesis submitted in partial fulfillment of the requirements for
the degree of Master of Science in Electrical Engineering in
the College of Engineering at the University of Kentucky

By
Jianhao Chen
Lexington, Kentucky
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2013

ABSTRACT OF THESIS

INVESTIGATION OF CdS NANOWIRES AND PLANAR FILMS FOR ENHANCED PERFORMANCE AS WINDOW LAYERS IN CdS/CdTe SOLAR CELL DEVICES

Cadmium sulfide (CdS) and cadmium telluride (CdTe) are two leading semiconductor materials used in the fabrication of thin film solar cells of relatively high power conversion efficiency and low manufacturing cost. In this work, CdS/CdTe solar cells with a varying set of processing parameters and device designs were fabricated and characterized for comparative evaluation. Studies were undertaken to elucidate the effects of (i) each step in fabrication and (ii) parameters like thickness, sheet resistance, light absorptivity solution concentration, inert gas pressure etc. Best results were obtained when the thickness of CdS planar film for the window layer was in the range of 150 nm to 200 nm. Also, CdS nanowires were fabricated for use as the window layer in CdS-CdTe solar cells. Their materials characteristics were studied with scanning electron microscopy (SEM) and X-ray Diffraction (XRD). Spectral absorption measurements on the planar CdS films and nanowire CdS layers were performed and results compared. It was established that the nanowire CdS design was superior because its absorption of sunlight was far less than that of planar CdS film, which would lead to enhanced performance in the CdS-CdTe solar cell through higher short circuit current density and higher open circuit voltage. Diode behavior of CdS-CdTe devices on planar CdS and nanowire CdS was analyzed and compared.

KEYWORDS: Thin Film Solar Cell, Nanowire, UV Absorption, Open-circuit Voltage, Close Space Sublimation

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April 16th 2013

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1.1 Renewable Energy

With growing consumption of energy and limited storage of fossil resources, development of renewable energy becomes more and more important. Its contribution to the world energy consumption has increased by 39 percent from 2000 to 2010, while the world total energy consumption has increased by 30 percent[1]. Based on the projection (Figure 1.1) of Energy Information Administration (EIA), it is noted that in the future energy development renewable energy will be the only source that remains increasing of its fraction among all sorts of energy resources, excluding liquid biofuels (the blue partial between renewable energy and natural gas in Figure 1.1). The fraction of renewable energy will increase to 11% from 7%. While the fossil resources keep dominating this planet and emitting greenhouse gas, renewable energy is slowly creating an opportunity to live a clean life without burning fossil resources.

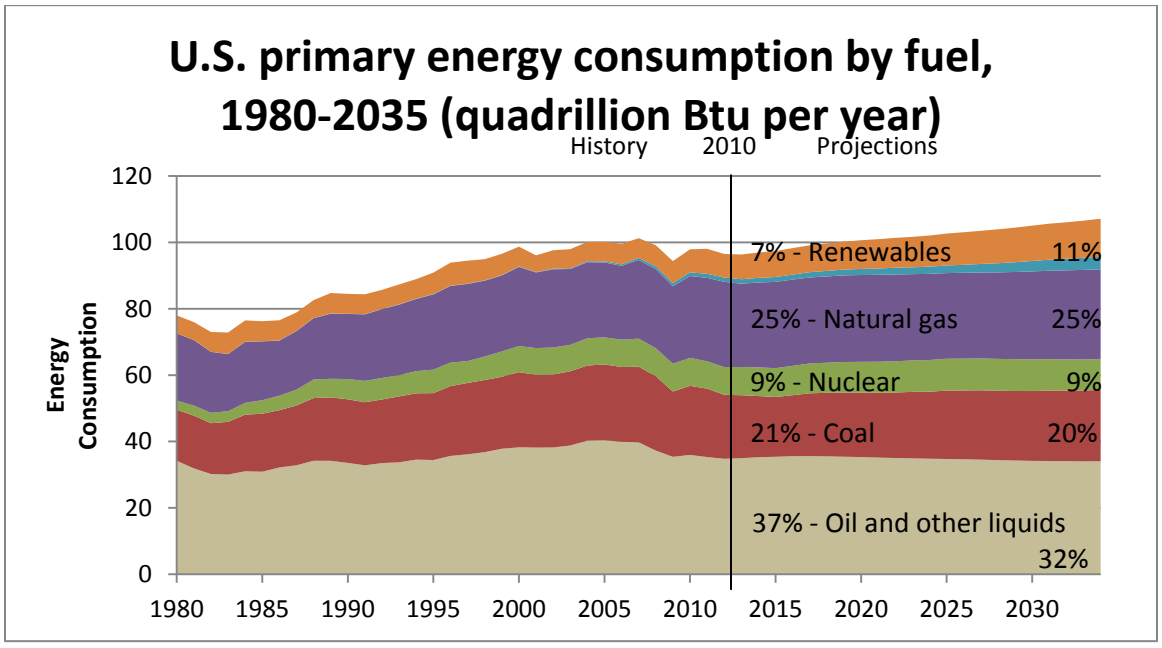

Figure 1.1 US primary energy consumption by fuel, 1980-2035
Data source: AEO2012 Early Release Overview of EIA

Hydro power, wind power, solar power and geothermal power are the major forms of renewable energy sources. Currently, hydro power is the most widely used renewable power in United States and the whole world. However, due to its huge potential impact to environment and climate, its development encountered most protests and has been limited to the minimum: for almost 50 years since 1960s there is no further progress [2]. On the other hand, wind power and solar power achieved explosive development during the past ten years[3]. As shown in Figure 1.2, photovoltaic module shipment has been increasing rapidly in the past ten years.

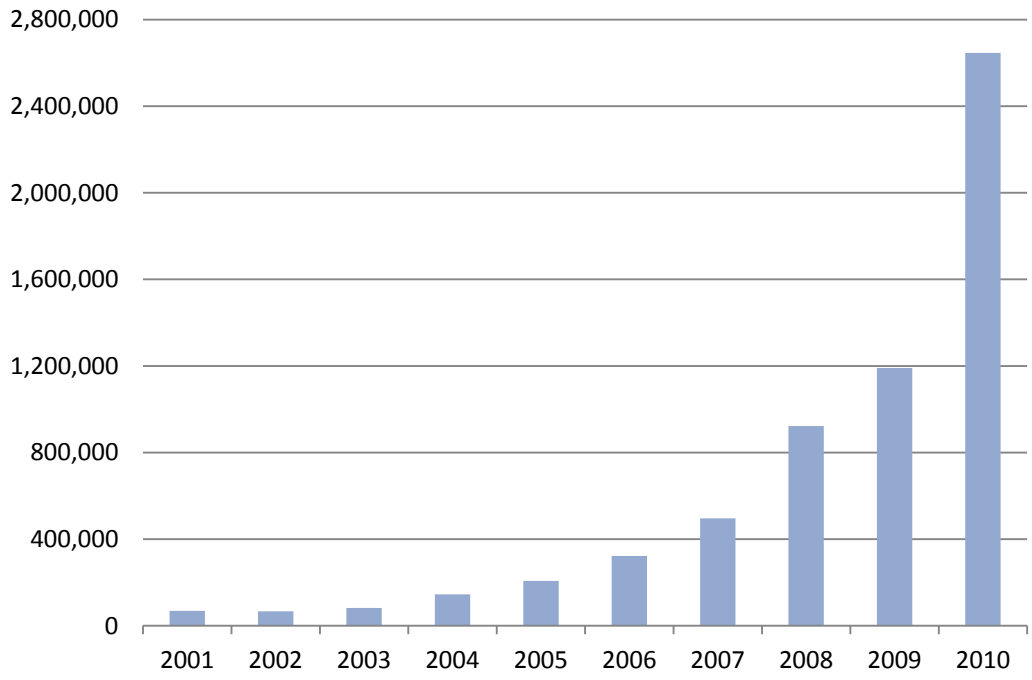

Figure 1.2 Annual photovoltaic module shipments, 2001-2010 (peak Kilowatts)

Source: U.S. Energy Information Administration (EIA), Form EIA-63B, Annual Photovoltaic Cell/Module Shipments Report.

However, the irrational development of solar industry brings crisis and green energy bubbles which were suddenly pricked in 2012. The solar panel market demand is not increasing that fast as people imaged due to the economy crisis after 2008 while the

manufacturing industry of photovoltaic devices are hugely invested by governments to stimulate the weak economy. Serious surplus production capacity is the most important reason that caused the bankruptcies of numerous photovoltaic companies and solar thermal power enterprises. At the mean time, immature technologies can neither lower manufacturing costs nor increase product benefits to help relief the pressure of bad market situation. Considering these factors, our research on new technologies of thin film solar cells have more significant meanings and contributions to future photovoltaic market.

1.2 Solar Power

Solar power industry is developing rapidly even though slightly impeded by 2008 financial crisis. There are two ways to convert sun power to electricity, either installing photovoltaic cells or utilizing solar thermal techniques. Based on photoelectric effect, a photovoltaic cell can convert sunlight into electricity directly instead of being transferred into thermal power. Solar thermal, also named concentrated solar power, uses mirrors or lenses and track systems to focus sunlight to get thermal energy, and then converts heat power to electricity. This thesis do focuses on photovoltaic cells only, and more information of photovoltaic cells is given below.

Solar power is ranked third after hydro and wind in renewable energy and recognized as the one of the feasible power sources in the future for our planet. Solar panels are formed to generate enough power for residential use. A solar panel is constructed by solar modules, and one module is constructed through numerous cells connected in parallel. Combining all power from individual cells, a panel can provide usable DC electric.

A solar cell is fabricated basing on semiconductor theories and consists of P layer, N layer and P - N junction. At present, the most common solar cell material is silicon. Crystalline silicon module is the most widely used module in market while some thin film modules are attracting more and more attentions at present such as CIGS (Copper

Indium Gallium Selenide), amorphous silicon, microcrystalline silicon and so on. Currently, the largest solar power plant is Agua Caliente Solar Project in Arizona with capacity of 397 MW[4]. However, this record will be broken in few years since numerous huge projects are in planning or under construction, of which many have capacity larger than 400 MW and even several have capacity more than 1000 MW. Among present largest solar power plants, almost all of them relied on silicon panels except for some utilized CdTe (Cadmium Telluride) materials. Till 2012, Sarnia Photovoltaic Power Plant in Canada is the largest CdTe power plant in the world, with 97 MW capacity constructed by the world's largest CdTe panel manufactory First Solar.

Compared with traditional power plants, a solar power plant takes much less time to complete. As the development of solar techniques and consideration of construction cost, thin film solar panels are growing more quickly and challenging traditional crystalline silicone. CdTe is one of the most promising materials to make high efficiency thin film solar panels.

1.3 Thin Film Solar Cell Introduction

A thin film solar cell is fabricated through depositing several thin layers of photovoltaic materials on a substrate. The thickness of a thin film ranges from a few nanometers to tens of micrometers. Thin film solar cells can be fabricated from amorphous silicon (a-Si), copper indium (gallium) diselenide (CIGS), cadmium telluride (CdTe) and organic materials.

In the future, the most promising future PV panels will be constructed of thin film materials. Certain materials have the advantages like, direct bandgap with energies near the peak of the solar spectrum, relatively high absorption constants and the capability of being fabricated with multi-junctions. Comparing with single crystal devices, there are limitations to carrier mobility and subsequent lower device performance. However, laboratory conversion efficiencies for single junction (as shown in Figure 1.3) over 25% have been achieved.

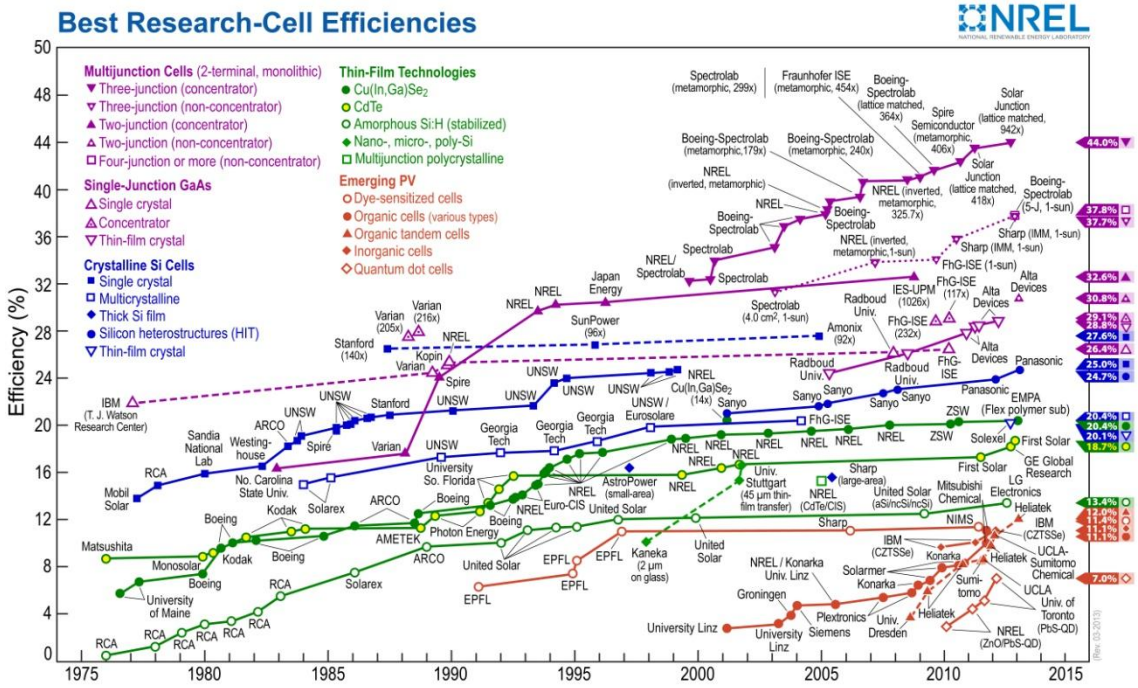

Figure 1.3 NREL compilation of best research solar cell efficiencies

Source: NREL website, http://www.nrel.gov/ncpv/images/efficiency_chart.jpg

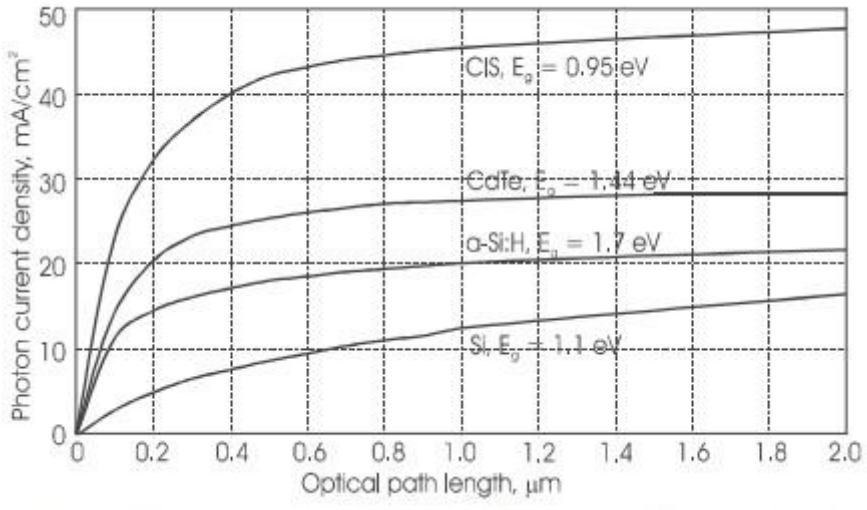

Figure 1.4 Photon Current vs. Optical Path Length for Thin Film Materials, Compared with Crystalline Silicon, Standard Test Conditions[5]

Thin films solar cells are less expensive because only a minimal amount of material is required to deposit a film layer with a thickness of 1 or 2 micrometers. Figure 1.4 shows the photon current vs. optical path length for common thin film materials: amorphous silicon (a-Si), copper indium diselenide (CIS), cadmium telluride (CdTe). Note that all of the thin film materials approach photon current saturation within 1 μm, whereas crystalline Silicon requires significantly greater thickness for full photon absorption.

Thin Film silicon solar cell is made from amorphous silicon, which has a direct band-gap with an energy gap larger than pure silicon. Hence amorphous silicon solar cells have a much better absorptive capacity than crystalline silicon and have the peak absorption at a wavelength closer to the peak of the solar spectrum. In addition to above introduced advantages, to make amorphous silicon a suitable material for thin film cells, fabrication difficulties should be solved. Fortunately, the instability mechanism in amorphous silicon is reasonably well understood and means for overcoming the instability are now in common use. On the other hand, additional efficiency increases have been achieved for amorphous silicon by the use of multi-junction cell structure.

Due to a direct band-gap of 1.43 eV, GaAs (Gallium Arsenide) becomes an attractive PV material. As most thin film materials, it also has a relatively high absorption constant. However, GaAs is limited by its high production costs. Production of pure GaAs requires the productions of pure gallium and pure arsenic. Modern GaAs solar cells usually consist of thin films of which GaAs grows on substrates such as Ge through thin film deposition processes.

In 1974, the first CIS (Copper indium diselenide) solar cell was reported by a group at Bell Laboratories[6]. CIS was considered as a potential photovoltaic material due to its attractive direct bandgap of 1.0 eV, the very high optical absorption coefficient and ideal inexpensive fabrication processes. Furthermore, the cell components are available in adequate quantities and processing technologies of the manufacturing, deployment and decommissioning fall within acceptable environmental constraints. Silicon has been studied intensely for decades and is well-understood by the scientific community, while

CIS are less understood. As long as more experiments and researches were conducted on CIS and its fundamental properties were discovered, chances for significant device enhancement will be achieved.

Theoretically, CdTe solar cells have a maximum efficiency limit close to 25%. With a favorable direct band gap and a large absorption constant, the material is receiving more and more attention. Comparing with other thin film materials, CdTe plays a much more important role in photovoltaic industry. As early as 2001, 16.8% efficiencies were being achieved for laboratory cells, and highest industrial module efficiencies had reached 11% for large area (8390 cm^2) module[7]. At present, the newest CdS/CdTe solar cell efficiency record is 18.7% achieved by First Solar in March, 2013. The record of module efficiency is set by the same company at 16.1% which is much higher than the last record of 14.4%. New open circuit voltage record is also recorded at 903.2 mVolts [8]. Even though CdTe thin film solar cells were challenged by the available quantities of components on earth, Cadmium and Tellurium are both sufficient for the production of many gigawatts of arrays. The amount of cadmium poses a possible fire hazard and some concern at the time of decommissioning of the modules. As the toxicity of Cadmium and Tellurium, CdTe cells should be completely recycled. Fortunately, the cost for recycling CdTe modules is less than $0.04 per watt, together with the recovery of glass, CdCO3 and clean EVA[9]. Nowadays, CdTe is the only thin film material that is able to surpass crystalline silicon in cheapness for constructing a significant solar power site. All large scale solar power sites all over the world were either utilizing crystalline silicon panels or installed with CdTe modules.

1.4 Theoretical Fundamentals of Solar Cells and Related Semiconductor Principles

In general, a photovoltaic device has a structure as shown in Figure 1.5. N - type layer provides electrons and P - type layer provides holes to enable charge carriers flow through the whole device. A junction between N and P type materials will be formed with

an electric field to balance the current generated by the diffusion of electrons and holes. When sunlight shoots on N type material, more electrons were created and the balance between N and P will be broke and hence electrons move from N to P and a current from P to N will be observed. Unless an electron travels to P type successfully, solar energy will be transferred to heat instead of electricity. Thus junction is the key part for electric power generation. To reduce the electron-hole recombination losses, material purity of any layer is highly-emphasized. And N type layer is made as thin as possible to reduce the length of light generated hole's traveling path.

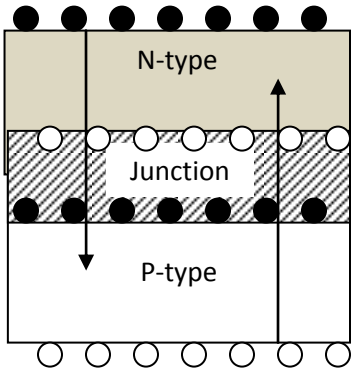

Figure 1.5 Structure of a Common Photovoltaic Device

Contact layer is deposited on P type to achieve better surface conductivity and to reduce sheet resistance (of which detailed influence on solar cell performance and related experiments were illustrated in Chapter 3). The material chosen to form the contact is very crucial. Right material may enhance solar cell's performance and bad filling will set barriers to impede the carrier exchange. Take silicon solar cell as an example, the back contact covers the entire cell and is commonly made of evaporated aluminum and then annealed after evaporation. Aluminum atoms would diffuse slightly into silicon during the annealing process and hence create a strong bond that will not break under thermal cycling. Also a more positive layer, P+ layer, will be formed (shown as in Figure 1.6) since aluminum is a group III element which acts as a p-type donor and produces a heavily doped p-region. This heavily doped p-region creates an impurity gradient that produces a resulting electric field that accelerates holes toward the back contact.

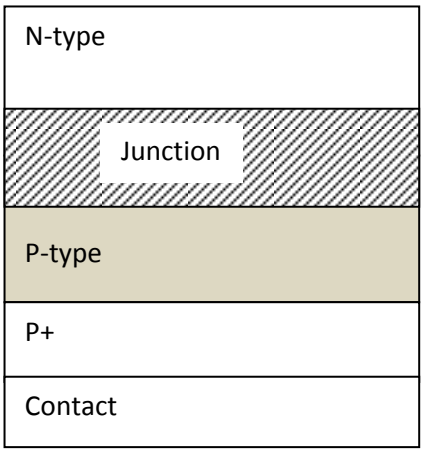

Figure 1.6 Structure of a Photovoltaic Device with P Layer Heavily Doped

For a CdS/CdTe solar cell, to satisfy the requirement of ohmic contact, graphite was used as contact material instead of metals. To form a p+ layer, some metal, such as copper, was deposited before the fabrication of back contact. Or, N. Romeo, etc. proposed to use Sb_2Te_3[10] as contact component which is a p+ type semiconductor without additional deposition of other metal material into p layer. Hence, CdTe layer was kept with high purity and none recombination particles were introduced to semiconductor, eliminating the potential challenge of diffusion of impurities into junction through gaps between grown crystals. Basing on numerous experiments, this problem is commonly found and has rare effective solutions.

Chapter 2 CdS/CdTe Solar Cell

2.1 Traditional Planar CdS/CdTe Solar Cell

CdTe is short for Cadmium Telluride and used as the P type material of CdS/CdTe thin film photovoltaic device. This thesis has analyzed properties of CdS and its role in fabricating CdS-CdTe thin film solar cells and enhancing the power conversion efficiency of the photovoltaic device.

CdTe has a direct band gap of 1.49ev, which is larger than silicon with 1.1ev and perfectly matching the sunlight spectrum. Its absorption coefficient is as high as 10^5 cm^{-1} and several micrometers of a CdTe film is able to absorb 99% of photons with energy above this band gap[11]. CdTe solar cells fabricated in laboratories have reached a new high efficiency record of 17.3%, confirmed by NREL in 2011. For large scale use, the best module efficiency is 13.5%, published by the largest CdTe solar panel manufactory, First Solar[12].

A thin film solar cell is normally consisted of several thin layers with thickness ranging from a few of nanometers to dozens of micrometers. A typical CdTe cell structure is shown in Fig 2.1. Sun light shines on the glass substrate; goes through transparent conductive oxide (TCO) layer; and then absorbed by P type layer CdS and N type layer CdTe. Sun light photons are either absorbed in CdS/CdTe junction and CdTe layer or transferred to thermal energy. The materials for making back contacts are copper or a mix of copper and graphite. TCO layer is usually deposited with Tin Oxide or Indium Tin Oxide (ITO). In order to improve the transmittance and reduce the sheet resistance of TCO layer, films made from other materials like Cd_2SnO_4, Zn_2SnO_4, $CdIn_2O_4$, $Zn_2In_2O_4$[131415161718] and etc. are under researching. In this paper, all experiments mentioned were conducted on glass substrates with the TCO layer made from traditional material of ITO/SnO_2.

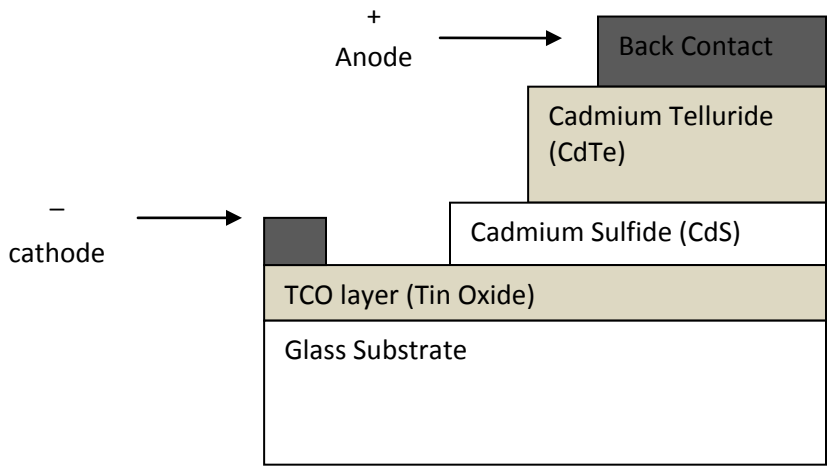

Figure 2.1 Typical CdS/CdTe Solar Cell Structure

2.2 Nano-wire Solar Cells

Because nano-scale materials possess special characteristics and often bring surprised improvement to general products, nano-structures are now being investigated for their potential enhancements in photovoltaic devices. Goals of applying nano-techniques in solar cells are to lower manufacturing cost and to obtain higher power conversion efficiency. Comparing with traditional solar cells, much less materials are used in nano-structured devices and hence inexpensive solar cells are made with much thinner films. A nano-structured solar cell can have an absorber layer (P side of the semiconductor device) with thickness as thin as 100 nm, which was successfully fabricated in our lab (Electronic Device Research Lab, EDRL) in 2012, even thinner than traditional thin film solar cell with thickness of several micrometers. To obtain higher energy transfer efficiency, comparing with traditional planar solar cells, nano-structured solar cells are hoped to gain advantages in following three ways. First of all, nano-structure can create multiple reflection for light in films and result in longer effective optical path for absorption than actual film thickness. Second, recombination effect in semiconductor junction is effectively limited and energy losses are reduced due to thinner films and hence a shorter path is available for light generated electrons and holes to pass

through. Third, the absorber and window layers of solar cell can be more flexibly designed since the energy band gap of various layers is able to be fabricated to desired value by varying the size of nano-particles. More and more attentions have been attracted by nano-structured solar cells and numerous new models have been proposed.

2.2.1 Nano-structured CdTe Homo-junction Solar Cell

Nano-structured CdTe solar cells with P-N homo-junction, of which both N type and P type were made from CdTe material (the structure was shown in Figure 2.2). Nanowires and nano-crystals were the typically used nano-structures. Determined from Tauc's relation, solar cells made from this structure have an effective band gap of 2.8 eV[19] which is much wider than a bulk CdTe solar cell with band gap of 1.5 eV. This enhancement makes CdTe a good candidate for window layers in homo-junction solar cells. CdTe nano-crystals were prepared by microwave-assisted synthesis and films were cast from colloidal solutions containing nano-CdTe particles. To observe the very tiny nano-structures clearly, nano-scale techniques were used to characterize and measure the thin films. Technologies and equipment, such as optical absorption, photoluminescence spectroscopy, profilometer, scanning electron microscopy, X-ray Diffraction and etc., were wildly used in modern thin film laboratories and industrial enterprises and many of above listed technologies were utilized in projects presented in this paper.

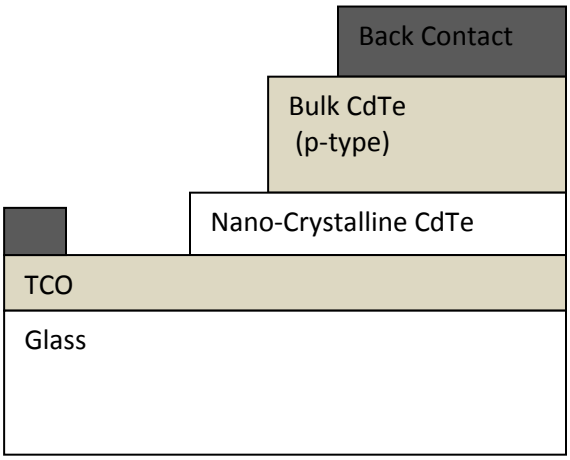

Figure 2.2 Device configuration of a CdTe homo-junction photovoltaic device

2.2.2 Nano-structured CdS/CdTe Hetero-junction Solar Cell

Nano-structure of Cadmium Sulfur (CdS) films were applied in photovoltaic device to form the hetero-junction with bulk CdTe layers. Nano-structured CdS can be fabricated in the formations of crystalline, porous and fibers. They have similar structures of thin film solar cell, but made from very different CdS processing procedures. Various experimental approaches to fabricate nano-structured CdS have been published about implementation of a variety of nano-scale techniques, like film deposition means of sputtering, E-beam evaporation and Closed-space Sublimation (CSS) and crystal growth methods of Direct Current (DC) electrochemical [20] in template synthesis, catalytic Chemical Vapor Deposition (CVD) growth[21], and etc. Nano-crystalline CdS films can be made from solution growth, chemical and microwave-assisted synthesis. Nano-porous CdS films are fabricated from ultrasound irradiation and nano fiber forms (known as nano-tube or nanowire) can be generated from a combination of ultrasound and chemistry solution deposition[12]. The structure of nanowire CdS received most of the attentions on nano-structured photovoltaic devices due to its optical advantages and large potential energy conversion efficiency. The typical structure of a solar cell with nanowire CdS films is shown in Figure 2.3. Sunlight directly shoots on glass substrates and photons are

absorbed in CdS nano fibers and P type CdTe layer. To control the growth of CdS nanowires, the electrochemical synthesis in templates[22] has been considered as one of the most efficient methods. Through this, the CdS nanowires generation was controllable through time duration and values of current and deposited CdS nano-wires were perfectly mounted in the direction perpendicular to the substrate surface.

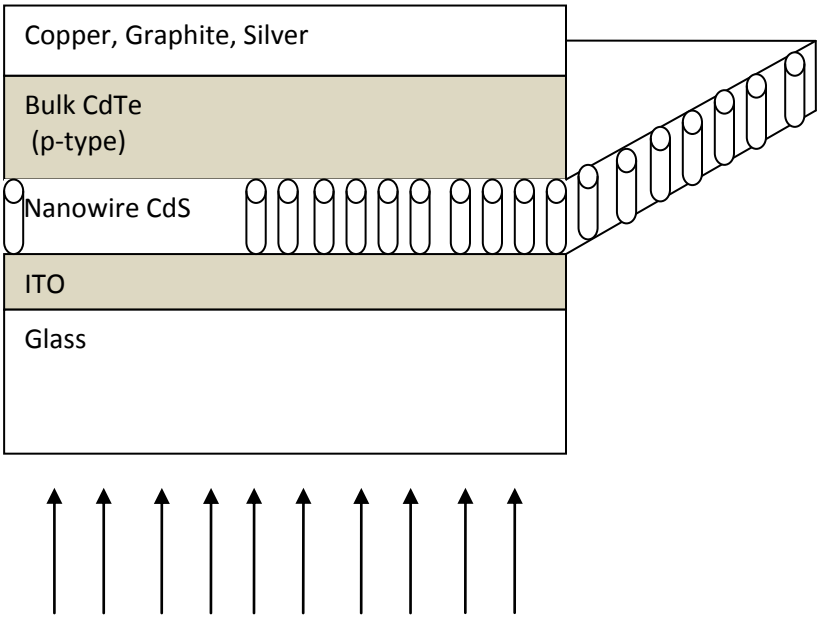

Figure 2.3 Structure of CdS Nanowire Solar Cell

In the ideal nano-structured CdS photovoltaic device configuration, CdS film thickness equals to the thickness of the junction formed by CdS nanowire and CdTe layer. Comparing with the junction of traditional thin film solar cells, the CdS–CdTe interface of nano-structured solar cell occupies only half to quarter of the junction area[23]. As junction reduced, the effective reverse saturation current (I_0) is decreased. Therefore, as quantified by equation 2-1, a higher open circuit voltage (Voc) is obtained.

$$V_{oc} = \left(\frac{AKT}{q}\right) ln\left(\frac{I_L}{I_0} + 1\right) \qquad 2\text{-}1$$

Actual improvement of the open circuit voltage depends on the effective value of the diode ideality factor A, as indicated in equation 2-1, which is characterized by the ratio of the optical area and the junction area and the prevailing dark current at the CdS–CdTe interface. In general dark conditions of hetero-junction solar cell, the dominant junction current is caused by the interface state recombination. On the other hand, if dark current is caused by electron-hole diffusion, only small enhancement of Voc will be achieved. Also, because photons, which pass through aluminum oxide instead of CdS films, will still get absorbed in the CdTe layer, the effective area for light absorption remains the same.

The nanowire-CdS layer has higher transmitivity than the traditional planar CdS window layer. It has been observed by EDRL researchers that the absorption peak of CdS nanowires is slightly shifted towards the blue region of the sun light, from 512 nm for traditional thin film CdS solar cells to 480 nm for nanowire CdS solar cells.[24] Therefore, more photons were absorbed by CdTe layer and light generated current is increased.

Additionally, due to higher optical transmission of aluminum oxides, overall transparency of the device is further increased and more photons can reach the CdTe layer and get absorbed.

Theoretically, for a nanowire CdS layer with thickness of 200 nm the light-generated current can be increased by 17% and an improvement of 8.4% for Voc is calculated. Since the power conversion efficiency of the solar cell is proportional to Jsc and Voc, an overall improvement of 26.8% in power conversion efficiency is expected.

The nano-structured solar cells in this paper were fabricated in nanowire structure and produced by DC electro-deposition in porous aluminum anodic oxidization (AAO) templates. Detailed experimental processes of nanowire CdS solar cells were illustrated in Chapter 4.

Chapter 3 Fabrication of CdS/CdTe Solar Cells with Planar CdS Films

The fabrication procedures presented in this chapter were for laboratory experimental work only. Industrial enterprises were utilizing very different methods which were kept in secret because of patent protection. All of listed projects in this chapter were conducted in EDRL(Electronic Device Research Lab) of Department of Electrical and Computer Engineering, University of Kentucky and CeNSE (Center for Nano-scale Science and Engineering) of ASTeCC (The Advanced Science and Technology Commercialization Center), University of Kentucky.

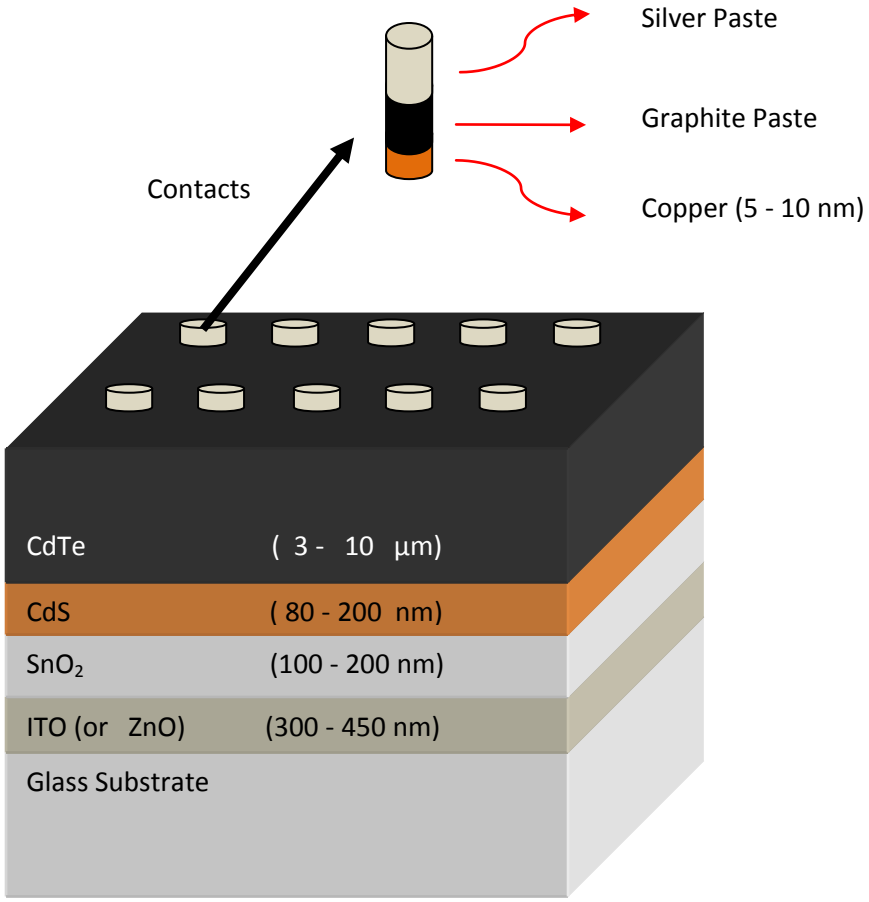

Figure 3.1 CdS/CdTe Thin Film Solar Cell Sample Configuration

Solar Cell fabrication processes were very complicated and strictly. There are more than 10 steps to build a complete sample. From the detailed configuration of a planar CdS/CdTe solar cell (shown in Figure 3.1), seven different layers were deposited on glass substrates with thickness in nano-scale. Formation of each layer may require a few processes. Among all processes, purity is the most important factor and significantly highlighted. Researchers should make sure that, before or after any process is operated towards the solar cell substrate, its surface should be rinsed with DI (de ionized) water and then immediately blow dry with pure nitrogen gas. To ensure the cleanness of solar cell substrates before deposition of any thin layer, sonication wash in DI hot water or organic liquids was employed to certain procedures.

Corning 7059 glass were used as substrate glass in most laboratories and TCO (transparent and conductive oxide) layer has to be independently deposited. All projects associated with this paper were conducted based on glass substrates with ITO layer originally deposited when purchased. The efficiencies were measured under AM 1.5 condition through a sunlight simulator machine. The related electric data was collected by a power programmable system and processed through a designed Lab View program. Finally, values of all parameters including efficiency, open circuit voltage, short circuit current, current density, fill factor, shunt resistance, and etc. were calculated from a MATLAB program based on measured data. Used MATLAB program codes for the determination in this thesis were appended at the end of this paper.

3.1 Preparation of Solar Cell Sample Substrate

Substrates were cut from large ITO deposited glass. To make it convenient for follow-up fabrication steps, substrates were usually cut with square or rectangular sizes, respectively 1 inch × 1 inch, 1 inch × 2 inches or 0.75 inch × 1.5 inches.

Substrates were cleaned through a sonication washer for many steps and in various cleaning solutions. Before sonication, substrates were rinsed with DI water and blew dry in nitrogen to remove glass scraps on surface which were caused by glass

cutting. If noticeable stains were found, substrates should cleaned by sonication washer in solution of 1% Liquinox soap with hot DI water[25]. After DI water rinse, for the first sonication washing, substrates were placed in organic liquid of IPA (isopropyl alcohol, also isopropanol), of which the molecular formula is C_3H_8O. IPA is widely used as a solvent and as a cleaning fluid because it dissolves a wide range of non-polar compounds. Hence, it is used to clean numerous electronic devices such as contact pins, magnetic tape, disk head, laser lenses and etc. After 30 minutes sonic cleaning in IPA, substrates were dipped into Acetone fluid and cleaned for sonication washing for another 30 minutes. Like IPA, acetone is also an organic liquid with chemical compound of $(CH_3)_2CO$ and wildly used as a cleaning solvent. Acetone is a good solvent for most plastics and synthetic fibers[26] and is ideal for cleaning fiberglass tools. Because its low cost and volatility, acetone is also commonly used as a solvent for rinsing and cleaning laboratory glassware. After sonication wash in IPA and Anceton, substrates were put into DI water for 30 minutes of sonication washing for 3 times. Finally, glass substrates were rinsed with DI water and blew dry in nitrogen and stored in closed plastic petri.

3.2 ITO Layer and Influence of Sheet Resistance on Solar Cell Efficiency

The glass substrates were well prepared with ITO layer deposited. As the most used TCO (transparent conductive oxide) layer, ITO is short for Indium Tin Oxide and also named as i-SnO_2. Typically, a suitable TCO layer for thin film solar cells possesses characteristics of high transparency, low resistivity and good stability. Other available choices for TCO layer include Tin Oxide (SnO_2), Indium Oxide (In_2O_3)[27], Cadmium Stannate (Cd_2SnO_4) and etc.

In general, TCO layers for fabrication of photovoltaic devices request a high transparency better than 80% in the wavelength region of interest (400-860 nm), which consists majority of solar energy. Research on TCO layers is aimed to reduce the sunlight energy losses as much as possible. The transparency of ITO layer used in this paper is between 70 and 80 and shown in Figure 3.2. The real value of ITO transparency should

be higher. This curve is measured without using glass as experimental base because the substrates we ordered are all well TCO deposited and this curve actually tells the transparency which is combined by both of glass and ITO layer.

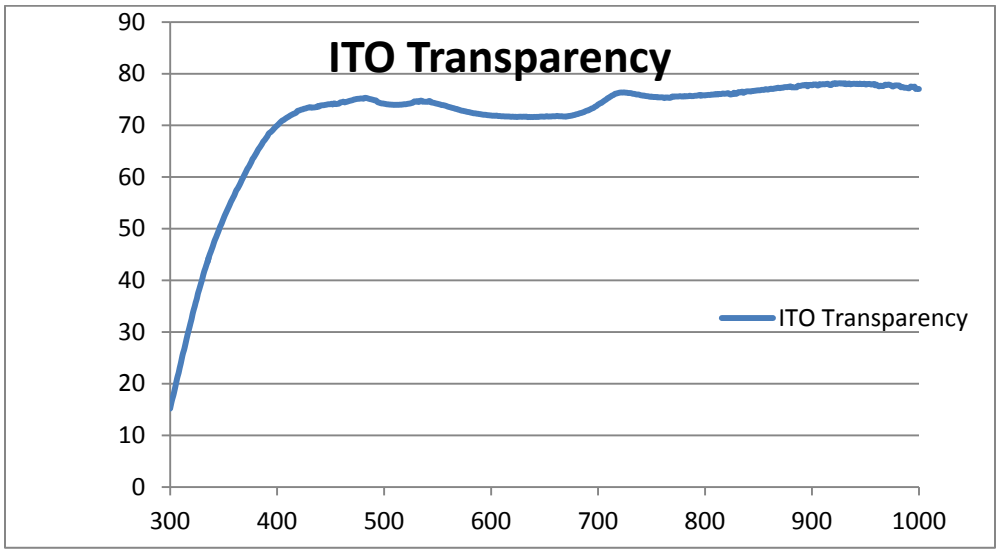

Figure 3.2 ITO Layer Transparency Measured from U-V Absorption for Cell 1 of HEP2

In most laboratories, the materials utilized for TCO layer usually have a low resistivity on the order of 2×10^{-2} ohmmeter or sheet resistance less than 10 ohm/square. The ITO glass used associated with this paper has a sheet resistance around 10~14 ohm/square. Table 3.1 shows the sheet resistance of HEP2 (High Efficiency Project #2) samples measured through four point probe method (see Figure 3.3) which avoids contact resistance. The equation for determining sheet resistance is as follows:

$$R_S = K_\rho \frac{V}{I} \tag{3-1}$$

K_ρ is a constant with value of 4.5324. It is observed from the table that minor plasma etch (a surface cleaning plasma induced skill) with power of 30 KW for 30 seconds does not change sheet resistance while surfaces of the substrates were etched in Oxygen. However, strong (60 KW) and long time (60 seconds) etches result in increase of the ohm/square value because plasma etch removes some ITO material while cleaning substrates by removing impurities on substrates surfaces. Since ITO layer itself is a very

thin film with a thickness of only 300 nm, the etch time should be controlled in less than 1 minute.

Table 3.1 Sheet Resistance of 6 Glass Substrates (unit: ohm/square)

Sample #	Before Clean	After lean by sonication	After 30 seconds Plasma Etch	After Deposition of SnO_2
1	13.4804	14.0482	13.6274	13.4535
2	13.5689	13.2937	13.5273	13.3056
3	13.3121	13.4695	13.6355	13.4405
4	13.5962	13.6816	13.7500	13.5600
5	13.3999	13.4146	13.4146	13.3039
6	13.3447	13.1476	13.3398	13.4156

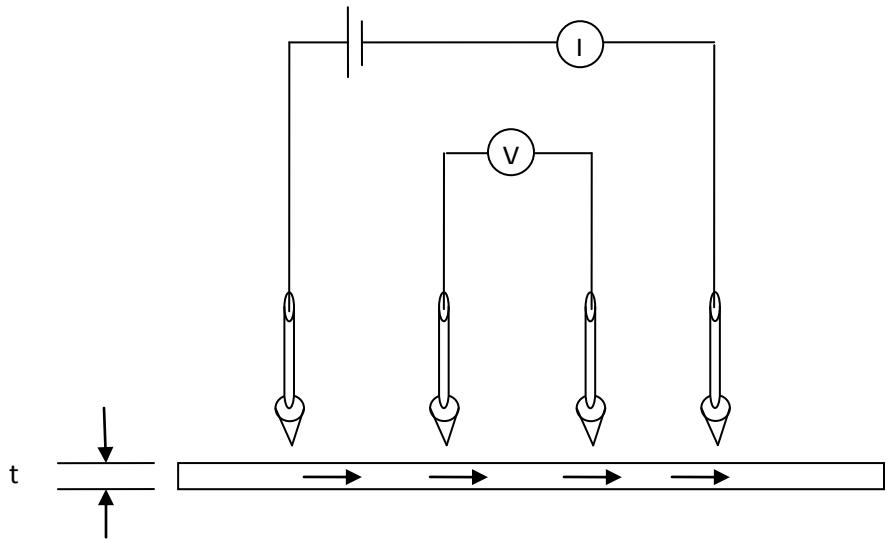

Figure 3.3 Four Point Probe to measure sheet resistance for a thin sample

During solar cell fabrication processes, especially the procedures for growth of CdTe layer, high temperature is necessary to deposit a good thin CdTe layer, good stability of TCO layer is certainly required at the high temperature (at least 500 ˚C). In other words, the diffusion of atoms from TCO into other subsequently deposited layers should be reduced to the minimum. It is strictly significant since CdTe film was made from CSS (close spaced sublimation) system which increases glass substrate temperature to more than 600 ˚C. To avoid the potential diffusion from TCO layer materials, a thin layer of SnO2 with thickness of 100 nm can be used as a barrier between TCO and other thin layers.

3.3 Deposition of Tin Oxide and Influence of Tin Oxide Annealing

Tin Oxide itself is a good material for fabricating TCO layer. It is quite stable and exhibits a sheet resistance between 10-20 ohm/square. In case that ITO may diffuse into the CdS layer, a very thin SnO_2 buffer layer (around 100-200 nm) is used as a diffusion barrier between ITO and CdS. Tin Oxide is deposited through sputtering skills which can form thin films uniformly and with accurate controllable thickness. High energy plasma on the SnO_2 material target activated molecules to hit on surfaces of bottom substrates. The sputtering technique can be utilized to deposit numerous materials in nano scale. Even CdS layer or CdTe layer can be made from sputtering and also it can be used to fabricate back contact layers.

Table 3.2 Change of Sheet Resistance of SnO_2 after Annealing

Sample #	Rs Before Annealing	Rs After Annealing
1	15.4102	90.1948
2	14.6850	90.5574
3	14.4130	90.5574
4	14.3224	90.6299
5	14.3167	90.6367
6	14.3586	90.6616

Annealing of Tin Oxide layer induced very high sheet resistance to substrates (experimental data is shown in Table 3.2) while interesting discovery was found that may enhance the open circuit voltage of fabricated solar cells due to this step. When CdS/CdTe solar cells have a very thin CdS layer or no CdS at all, i-SnO_2 layer can help to increase device performance. Generally, the CdS layer always dominates the device efficiency when the thickness is over 600 Å[28]. My experiment on Voc of HEP 1 project tells that when CdS thickness is larger than 600 Å, annealing of i-SnO_2 buffer layer can also improve values of open circuit voltage. Table 3.3 shows the Voc values measured after each important procedure. And Table 3.4 displays Voc values (for the same 6 samples used in Table 3.3) after formation of contact dots. Apparently, sample 1 with i-SnO2 layer annealed poses the highest Voc value. And it is more distinct after formation of contact dots.

Table 3.3 Voc of 6 samples for different procedures

Sample #	After CdTe Deposition	After CdCl2 Dipping and Annealing	After NP etch
1	388	475	633
2	336	494	572
3	438	409	589
4	437	432	576
5	359	433	612
6	471	422	591

* Sample 1 is the device that has i-SnO2 layer annealed

Table 3.4 Voc of 6 samples after making contacts (5 contact dots for each sample)

Contact #	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6
1	514	275	344	374	496	406
2	577	458	442	438	507	411
3	552	428	313	468	506	338
4	511	325	367	460	463	390
5	578	451	435	445	491	368

* Sample 1 is the device that has i-SnO2 layer annealed

In the other way, annealing of SnO_2 can enhance the absorption coefficient of the substrates. As shown in Figure 3.4, while all samples have very close photon transmission values during 500 - 700 nm of the light wavelength, the Tin Oxide annealed

sample shows brilliant performance in wavelength smaller than 500 nm or larger than 750 nm.

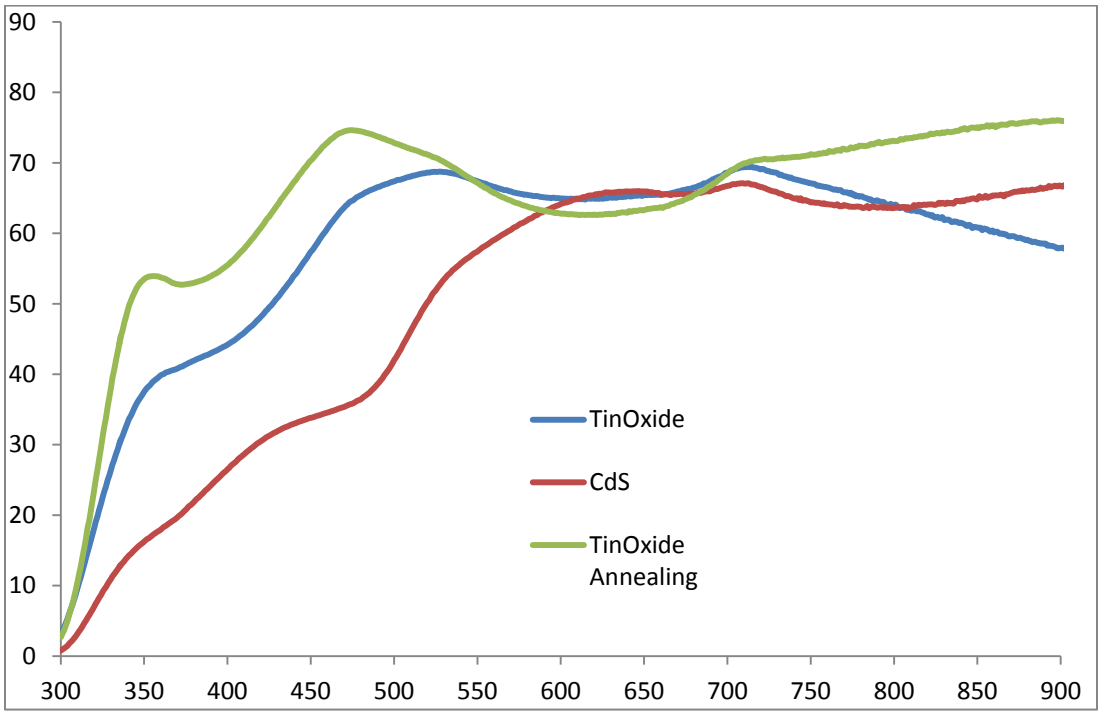

Figure 3.4 Transmissions of thin films

Though the advantages of annealing of i-SnO_2 layer is evident and encouraging, the induced large sheet resistance significantly decreases the current density and short circuit current of the device, resulting in very low device efficiency. Therefore, currently annealing of Tin Oxide is only under research in laboratories and no device with high efficiency made from this technique is reported.

3.4 Fabrication of CdS Films and Related Experiments

CdS can be deposited by numerous methods: deposition in air through metal organic chemical vapor[29], electrochemical deposition of material into the pores of anodic aluminum oxide films from an electrolyte containing Cd^{2+} and S in dimethyl sulfoxide[30], E-beam evaporation from a single crucible, sputtering through plasma hitting CdS target, close spaced sublimation with temperature above 400 ˚C, chemical bath deposition (CBD) with the whole films dipped in reaction solutions, and etc. A CSS system can deposit a few (1 to 3) substrates at a time and sublimated CdS may pollute the system components causing problems foe deposition of other materials. Through CBD, much more substrates can be deposited at a time (normally 6 to 10 substrates in a 500 ml beaker). The use of thermal evaporation can deposit more than 10 substrates at one time and its most remarkable advantage is that the CdS thickness is computer-controlled to 0.1 nm scale.

Chemical bath deposition is currently the most widely used method to deposit a uniform and thin CdS film. Before CdS deposition, the substrates were prepared with ITO layer and i-SnO_2 buffer film coated. While cleaning substrates in hot DI water through sonication, reaction solution was made basing on Table 3.5 in a beaker of 500 ml volume. To deposit 800 - 1000 Å of CdS, the constituents were outlined in Tab 3.5 induced into total solution volume of 200 ml. Solutions with 3 different constituents were introduced to the experiments and were compared of respective effects on photon absorption and cell efficiency among which solution 1 make the CdS films of largest thickness. The beaker is placed in a large glass dish filled with water on center top of a stirring heater. For the assurance of uniformity and quality of CdS film, substrates were hang in the solution kept in the center of solution (as shown in Figure 3.5) instead of leaning to the beaker wall in the bottom of the solution. A magnetic stir was continuously stirring in the beaker.

Table 3.5 Constituents for CdS by CBD

Chemicals	Solution 1 0.15M	Solution 2 0.05M	Solution 3 0.012M
NH4OH (ml)	5.4	4	5.45
CdCl2 (g)	0.73	0.368	0.30
NH4Cl (g)	0.72	0.268	2.675
Thiourea (g)	2.3	0.76	0.255
Time (Minutes)	8	10-15	38
Temperature (Degree C)	80-90	88	88

* Solution 1 is the one used for most photovoltaic devices presented in this paper.

** Solution 2 is the solution used in our lab in past years.

*** Solution 3 is from *D. Rose, 1999* [21] utilizing Ac chemicals instead of Cl chemicals.

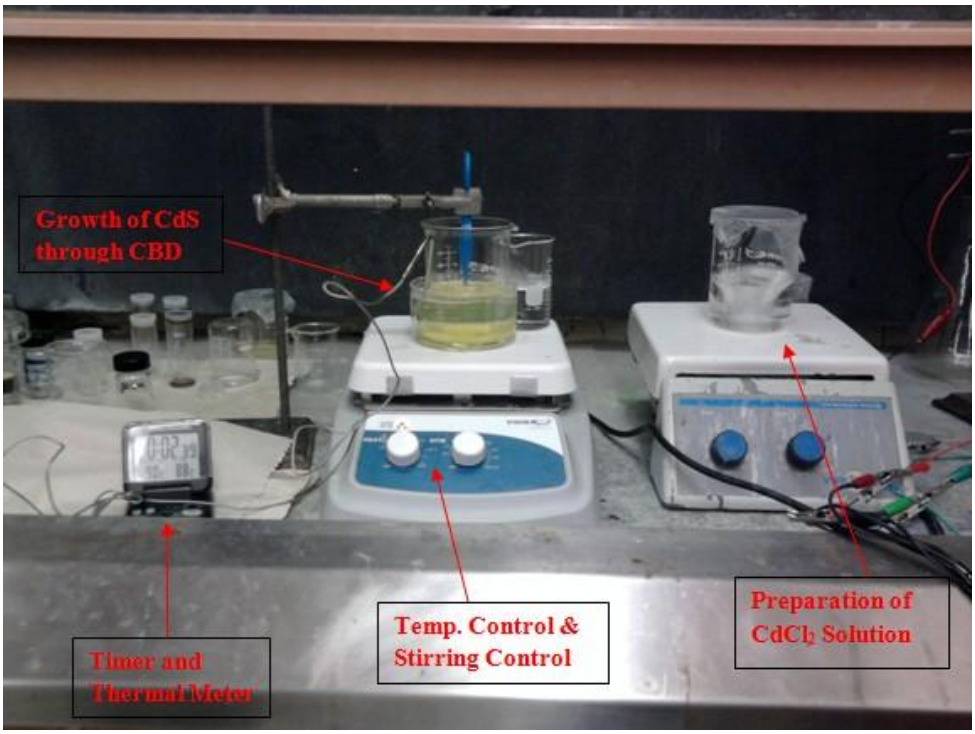

Figure 3.5 Photo of Fabrication of CdS

To make 200 ml solution, at first, $CdCl_2$ is added to 150 ml DI water and then allow 30 minutes to elapse so that the deposition temperature reaches 80 ˚C. The rest chemicals, NH_4OH and NH_4Cl are then added. Thiourea is added at last right before the deposition of CdS. Right amount Thiourea is dissolved in 20 ml water, together with DI water, to make the solution 200 ml. To minimize homogeneous reaction, thiourea solution is added very slowly through titration by four times. Also thiourea can be added once in total and the whole CdS deposition process is one dip. To make thick CdS films, more than one dip are conducted to substrates. As the temperature rises, reaction in the solution becomes strong and CdS grows more quickly.

Reactions in the solution is as follows,

$$CdCl_2 \Rightarrow Cd^{2+} + 2Cl^{1-}$$

$$NH_4OH \Rightarrow NH_3 + H_2O$$

$$NH_4Cl \Rightarrow NH_4^{1+} + Cl^{1-}$$

$$4Cd^{2+} + 4NH_3 \Rightarrow [Cd(NH_3)]_4^{2+}$$

$$SC(NH_2)_2 + 2OH^{1-} \Rightarrow S^{2-} + CH_2N_2 + 2H_2O$$

$$Cd^{2+} + S+ \Rightarrow CdS$$

After the total deposition time, substrates are removed from the bath immediately and then placed in warm DI water to do sonication until loosely adhered CdS particulates are removed. After blow dry in N_2, back side of substrates surface are wiped with dilute HCl to remove CdS films, also part of top side is wiped and thus this part of TCO layer is exposed for making electro-node. Once carefully wiped, substrates are rinsed with large amount of DI water instantly since CdS is very easily dissolved in HCl solution and the films may be significantly damaged with a very tiny dip on the surface. After removing extra deposited CdS films, a CdS batch is now successfully completed. Remaining chemical waste should be stored in hazardous waste containers dividedly and beakers should be cleaned with dilute HCl and then rinsed with DI water for several times. All

processes mentioned above should be conducted in a chamber hood in case of the toxicant material getting breathed by researchers.

3.5 CdTe fabrication through Close-spaced Sublimation System

CdTe exhibits a forbidden gap of 1.45 eV which is very close to the band gap for fabricating maximum of solar energy conversion. Because of its direct gap, its absorption coefficient is higher than $10^7 m^{-1}$ for energy larger than the forbidden gap, indicating that that only a few microns of material are enough to absorb all the light photons. A practical efficiency of 18.5% for CdTe solar cell was expected with an open circuit voltage of 0.880V and a short-circuit current density of 270 A/m^2 [31]. Methods of deposition of CdTe for laboratory use include vacuum evaporation, thermal evaporation, close spaced sublimation, and etc. Among those techniques, CSS made the highest efficiency solar cells ever and is most widely used in laboratories. Also CSS system is able to do $CdCl_2$ annealing if extra substrates support is available.

Before deposition of CdTe, substrates were dipped in CdCl2 solution (75% concentration in menthol) and then annealed in nitrogen under 400 ˚C for 15 minutes. This step is also necessary after deposition and will be illustrated in detail in next section. Subsequently, substrates were rinsed with DI water and blown dry in N_2. To clean the surface, samples were dipped into dilute HCl (1:40 HCl: DI water) for 5 seconds only and then immediately rinsed with lots of DI water. Substrates are well prepared for loading into the chamber of CSS system. The structure of CSS system is shown in Figure 3.6.

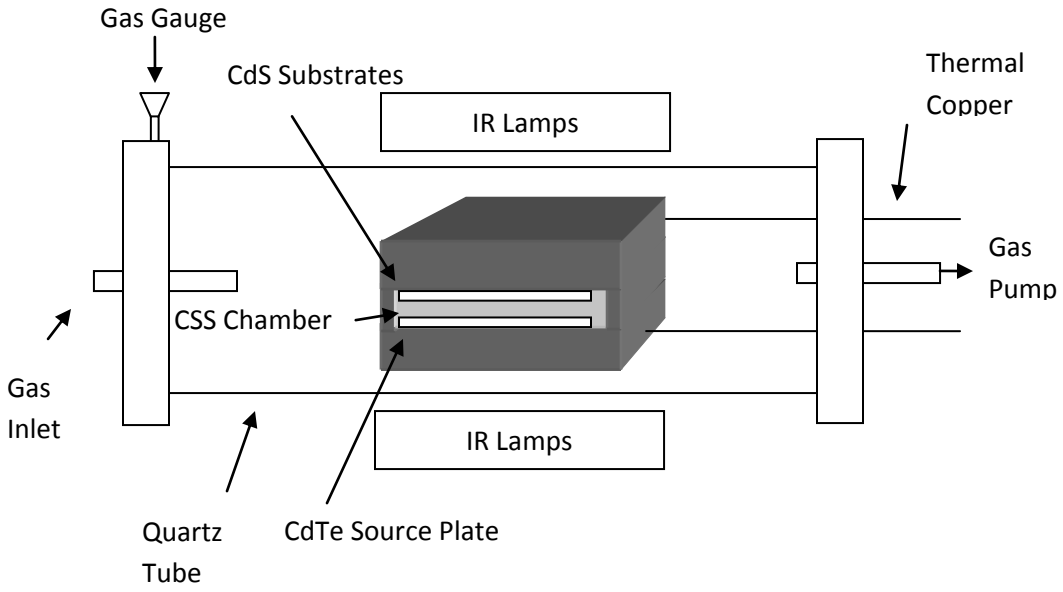

Figure 3.6. Outlne of the close-spaced sublimation system

During the CSS process, high substrate temperature is induced for fabricating better CdTe crystals and therefore obtaining higher efficiency. The ideal temperature is 680 ˚C or even higher, but normally substrates were set as a temperature close to 600 ˚C because of the limitation of the system. On the other hand, CdS may sublimate during high temperature and as consequently lower the limit the max substrate temperature. As observed by many groups, through CSS process, the CdS mixes with CdTe and produces ternary compounds of CdS_xTe_{1-x} and CdS_yTe_{1-y}.[32] The formation of these two ternary compounds is believed to be meaningful since it reduces the concentration of recombination centers. If CdTe is deposited at low temperature, the mixing process only happens during $CdCl_2$ treatment process. Thus, temperature is a very important factor to make CdTe film. To some extent, high temperature is essential to make solar cells with efficiencies above 15%.

To ensure the uniformity and quality of CdTe films, besides the application of high substrate temperature, a CdTe source is used instead of CdTe powder. The source is made from CdTe powder, with CdTe deposited on molybdenum foil with a film about 100 μm thick. The source is deposited in vacuum with 625 ˚C temperature for the CdTe

powder and 525 ˚C for the molybdenum foil. After molybdenum foil was well prepared, it is placed on the bottom of chamber which is made from graphite for withstanding high temperature. The glass substrates was placed on top of CdTe source with 2-3 mm space between them. Deposition can be done in vacuum or inert gas like argon or helium. Inert helium with pressure 2 Torr to 10 Torr was induced to the quartz tube due to the fact that in vacuum environment deposition rate is too quick to make uniform CdTe films. The timing of deposition starts when substrate temperature reaches 625 ˚C. In vacuum condition, it takes less than half a minute to deposit CdTe film of 3 to 6 μm, while in helium, it takes several minutes to about 15 minutes. Also, higher temperature brings larger CdTe crystals and hence resulted in higher efficiency.

As another key variable in CSS deposition besides of temperature, oxygen is added to the inert gas. It is found that at least 0.2 torr of oxygen (normally occupies 1.5% of mixed oxygen and helium) [33] is needed to ensure pinhole-free films when thin films are deposited at substrate temperature above 600 ˚C. Through improving the quality of the CdS/CdTe interface, oxygen enhances the creation of good junction and hence increases Voc. In addition, to prevent from decomposition of TCO materials (Indium Tin Oxide), oxygen protects against the harmful effects caused by high temperature. This effect was observed in a failed batch of solar cells in our lab. In spite of the advantages of applying oxygen, excessive oxygen may result in oxidation of CdTe source, especially in pressure over 10 Torr. To balance of advantageous and negative effects of oxygen on CdTe deposition, the total pressure is set as 2 torr.

3.6 $CdCl_2$ Treatment and Annealing

$CdCl_2$ treatment plays an important role in influencing the performance of the semiconductor device. All devices with more than 10% efficiencies have to rely on $CdCl_2$ treatment. Through dipping in the $CdCl_2$ solution, CdS or CdTe crystals grows larger based on following equation:

$$CdTe(s) + CdCl_2(s) \Rightarrow Cd(g) + Te(g) + Cl_2(g) \Rightarrow CdCl_2(s) + CdTe(s)$$

In theory, higher open circuit voltage comes along with larger crystals while over size crystal causes the instability of deposited films which was verified by experiments in EDRL. $CdCl_2$/methanol solution is used for treatment at temperature between 50 to 60 ˚C. $CdCl_2$ dissolves very easily in water but difficult to dissolve in methanol which takes more than one hour for the dissolving process even with a magnetic stir continuously stirring. $CdCl_2$ solution is heated over 50 ˚C but below 60 ˚C based on that the boiling temperature of methanol is 60 ˚C. Because methanol volatilizes easily, beaker of CdCl2 solution should be covered with an aluminum foil during all heating and treatment operating processes. Due to the toxicity of $CdCl_2$, all related operations should be taken in a gas outlet chamber. 15 minutes is required for dipping in the solution. After that, samples were put into a tube furnace that is purged with Helium, Argon or Nitrogen to do annealing for 15 minutes under 400 ˚C. Based on previous experiments, $CdCl_2$ solution with 75% concentration makes the highest efficiency device comparing with solutions of 60% or 90% concentration. To some extent, high concentration of $CdCl_2$ may have a bad impact on device. Exposure of CdTe films to $CdCl_2$ vapor can help make large crystal grains, however, over $CdCl_2$ treatment (too high solution concentration or too high annealing temperature) may cause problems of film adhesion and damage the devices. Through a face-to-face annealing project, over treatment is carefully observed and it is found that over treatment brought higher Voc temporarily before NP etch but resulted in a big drop of Voc and even film breaks after NP etch.

Because of its ability to eliminate of fast recombination centers in the CdTe films and reduce recombination centers in the junctions, $CdCl_2$ treatment is also taken after deposition of CdS to reduce recombination centers in CdS film and annealed in an inert gas purged tube to grow better CdS crystal grams. However, CdCl2 treatment for CdS is not necessary as many groups reported high efficiencies without this process.

After annealing, substrates should be rinsed with DI water to remove excess $CdCl_2$. Also some oxides are found on CdTe film surface which should be eliminated before making back contacts. Hence, the process of NP etch is introduced to remove the oxides.

3.7 NP Etch

During the processes of $CdCl_2$ treatment and high temperature annealing, some oxides were formed on the CdTe surface even inert gas was induced to annealing.

$$CdCl_2(g) + O_2(g) + CdTe(s) <=> TeCl_2(g) + 2\ CdO(s)$$

These oxides need to be removed before formation of contacts to achieve better conductivity and hence an acid etching is proposed.

To reorganize the CdTe surface, most research groups are utilizing wet etching which can achieve contaminant free materials surface, allows fast treatment time and is very easily to use. Dry etching is applied to industry in case interrupting the in-line production and for safety consideration. Most commonly used etchants are Br2/methanol solutions (BM) and aqueous nitric acid/phosphoric acid mixtures (NP). Other CdTe etchants are listed below as H2O2, hydrazine, thiosulfate, acidified dichromate, citric acid, ammonia and alkali metal hydroxides[34]. One treatment that has shown very good success at IEC, but also highlights the hazardous nature of these treatments, is the Br2-Dichrol-Hydrazine (BDH) etch[35]. These treatments transfer surface telluride ions, Te^{2-}, to elemental tellurium, Te^0, and dissolve Cd^{2+} ions from the film, which are unable to remain in a tellurium environment. Hence a Te surface was generated on top CdTe surface for contacts formation.

The mostly used NP etch solution is made from 1% HNO_3, 88% H_3PO_4 : 35% DI water or 1% HNO_3, 77% H_3PO_4 : 29% DI water. For making successful back contacts, etching of 20 to 60 seconds is required. Commonly the NP etch is ended around 30 seconds when the symbol that bubbles completely covering on CdTe surface appears. The formation of bubbles, which are generated due to the release of gaseous NO or NO_2 products, on the CdTe surface is observed after dipping of 20 seconds. The time for bubbles to appear varies from 15 to 30 seconds depending on temperature, solution concentration and the presence of surface oxides. As the NP etch is aggressive, it is expected to remove any tellurium oxides formed during treatment and annealing. Following etching, the CdTe surface is silvery-gray and roughened due to grain boundary

etching and a 50 – 100 nm surface Te layer[36] is generated. However, due to the aggressive nature of the NP etch this treatment can only be used for etching thicker CdTe layers (larger than 3 micrometers). Damages to films and reduction of Voc and FF have been observed in experiments when NP etch is taken on very thin CdTe layers. The thicker the CdTe layer is, the more improvement is obtained from NP etch.

Once the fact that bubbles cover whole CdTe film was observed, the substrate should be taken out immediately and rinsed with lots of DI water and then blown dry with Nitrogen. Unlike $CdCl_2$ treatment which requires immediate dry in Nitrogen without DI water rinse, NP etch may damage devices due to its strong causticity and possibility of diffusing into deep semiconductor layers through CdTe crystal gaps. In addition, after cleaning, back contacts were deposited on top of CdTe films instantly in case of oxidation of film surface. Thus, before NP etch, tools and materials for contact formation are usually prepared ahead.

Despite widespread and historical use of NP etch, its mechanism and dynamics on CdTe are not well understood. Experiments about influence of NP etch on solar cell performance will be introduced in Chapter Five.

3.8 Formation of Back Contacts

After NP etch the back contacts were deposited instantly to avoid re-generation of oxides. It is believed that copper is necessary for fabrication of back contacts, however, many other materials are now proposed to replace copper for back contact formation. ZnTe and Sb2Te3 can be made from vacuum evaporated; NiTe2 is deposited through solution deposition[37]; molybdenum is coated by sputtering or thermal evaporation (under experiments in our lab, EDRL); and antimony (Sb) has been used to replace copper[38].

Traditionally, back contacts are made from copper/graphite or copper/gold. It is difficult to make good contacts since copper often diffuses into junction and hence degrades the device performance. To avoid or minimize this influence, many methods

have been attempted. The easiest way is to use HgTe/Cu graphite paste to brush on CdTe surface. Normally it is made from stirring 4 grams of HgTe/Cu (about 2 atomic % Cu) powder into 10 grams of graphite paste. Because contacts by brushing paste are always too thick, the paste is thinned as needed with methyl ethyl ketone. Or copper can be deposited through sputtering or thermal evaporation, and then brushed graphite paste on copper top. Back contacts of all devices mentioned in this thesis are made from sputtering machine or thermal evaporation.

Aluminum foil with circular holes (area of 0.07 cm^2) are prepared before NP etch and used to cover CdTe surface before deposition of copper. The holes are made through a bradawl with flat head of 0.07 cm^2 area. Thus, copper will only be deposited on the exposed rounds. To minimize the diffusion of copper into junction, sputtering power or current of thermal evaporator is set at a very low value just allowing minor copper atoms deposited per second. The thickness of copper is controlled between 5 to 10 nm. After that, copper is annealed in inert gas, helium or argon, or in nitrogen under 150 ˚C for 15 minutes. Gas flow is kept going until solar cells are completely cooled and removed from the tube. Then graphite paste is brushed on top of round copper films and devices demands to be annealed again for 15 minutes under 120-150 ˚C. The last step is to put silver paste on graphite and the part of substrate glass with ITO exposed. Because Ag is dissolved volatile organic liquid and it is not necessary to anneal after Ag pasted and solar cells can be left dry in air. If annealing is applied after pasting of Ag, condition of 100-120 ˚C and 10-15 minutes are recommended.

3.9 Solar Cell Measurement

Till now, a complete solar cell is fabricated. Through a solar light simulator system, I-V or J-V curve is measured through a Lab View program. Before measuring, the system is calibrated with a standard silicon solar cell to confirm the AM 1.5 condition. Through a program written in MATLAB language, parameters including power efficiency, open circuit voltage, short circuit current, current density, sheet

resistance and shunt resistance are determined and respective curves are generated. The MATLAB code applied is presented in appendix.

Measurements used in above procedures include UV absorption for measuring transparency, four point probe measurer for determining sheet resistance, SEM (scanning electron microscope) for watching film surface images or measuring thickness of nano-scale film, X-ray scattering (XRD) for observing crystal parameters, thickness profilometer for measuring film thickness and observing surface uniformity etc.

A detailed procedure flow in show below (Figure 3.7).

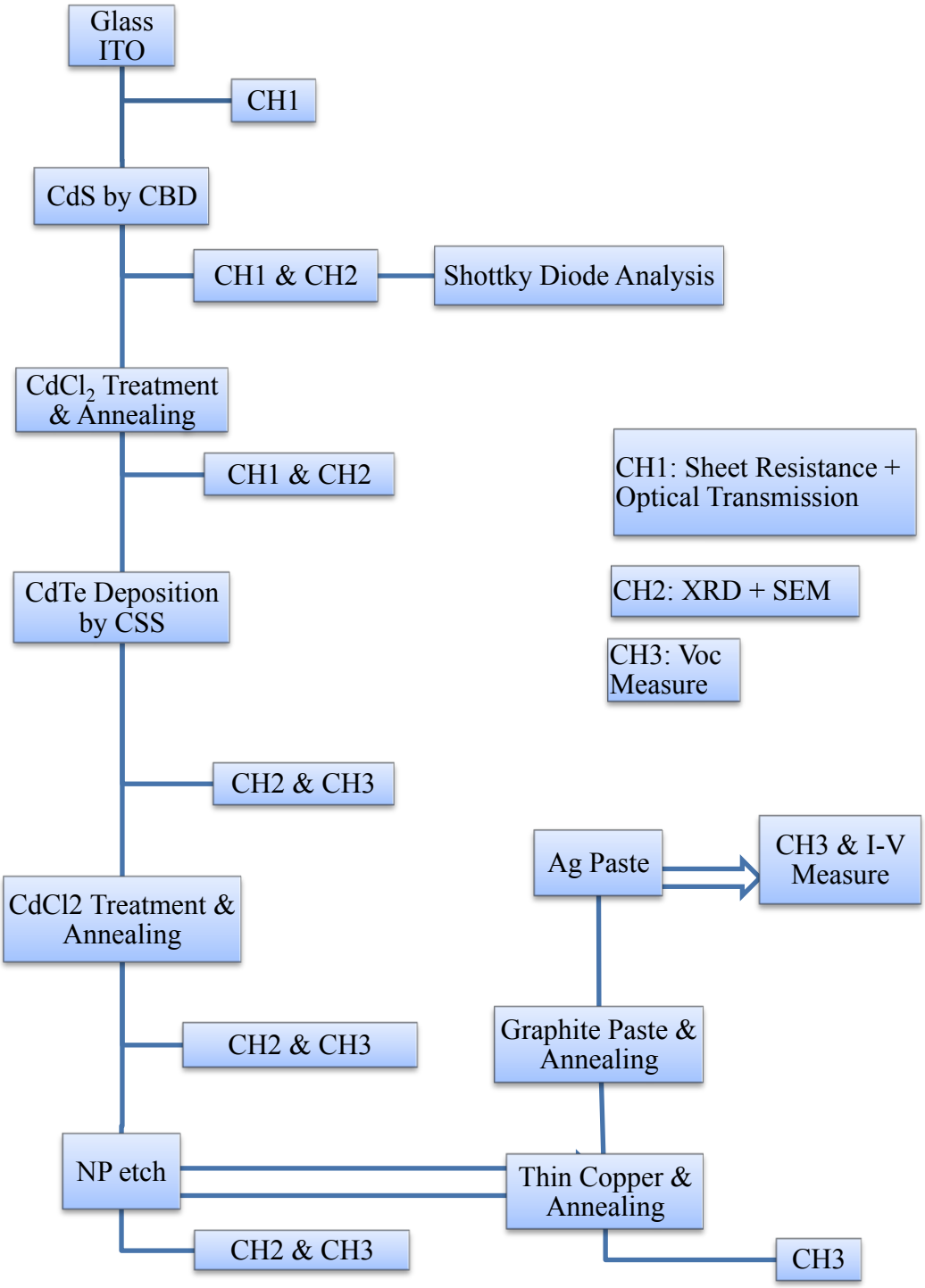

Figure 3.7 Operation Flow of Fabrication of CdS/CdTe Solar Cells

Chapter 4 Fabrication of CdS/CdTe Cells with Nano-wire CdS Films

The nano-structured solar cells have been attracting more and more attention around the world. Researches on nano-scale solar cells have are playing more significant roles at present under the serious bankruptcy of the traditional photovoltaic industry. Due to the price competition, benefits from solar cells manufacturing are almost gone. Solar cells made from nano-structures have much lower manufacturing cost than normal thin film solar cells and larger potential efficiency are expected. Consequently, it is reasonable to get more benefits from nano-structured thin film solar cells. As the most widely used thin film solar cell material, CdS and CdTe, their nano-scale structures are in research by many groups.

To make good nano-structure CdS films, well-aligned and well-distributed nanowire arrays as well as highly crystallized structures are necessary. Due to the requirement of uniformity and nearly parallel porous structures of CdS, AAO (anodic aluminum oxide) films are ideal templates when doing electrochemical deposition of the highly anisotropic, and aligned nanowire arrays[39,40]. Nano-wire CdS solar cells share many same processes with planar CdS devices including TCO layer deposition, CdTe films formation through CSS system and fabrication of back contacts. Electro-deposition of CdS nanowires and fabrication of AAO templates are the key processes in fabricating CdS nanowires. To make AAO nanowires, at first, 5 nm (has to be controlled under 10 nm) of titanium through sputtering is deposited on i-SnO_2 film. And then substrates are instantly coated with 100-200 nm of aluminum by E-beam evaporation in case of oxidation of the titanium. Anodization in 0.3 M Oxalic acid and etch in 5% phosphate acid for 45-60 minutes are applied to make nano-pores in the aluminum layer. After RIE (Reactive ion etching), CdS is deposited through dc electro-deposition and hence nanowires are fabricated.

CdTe deposition processes for nano-structure CdS/CdTe solar cells are the same as that applied to fabricate traditional CdS/CdTe solar cells with planar CdS films. A configuration and fabrication flowchart of nanowire CdS/CdTe solar cell is shown in

Figure 4.1. For flow 1, the AAO templates are preserved. For flow 2, the AAO templates are removed and CdS nanowires are mounting on conductive layer directly.

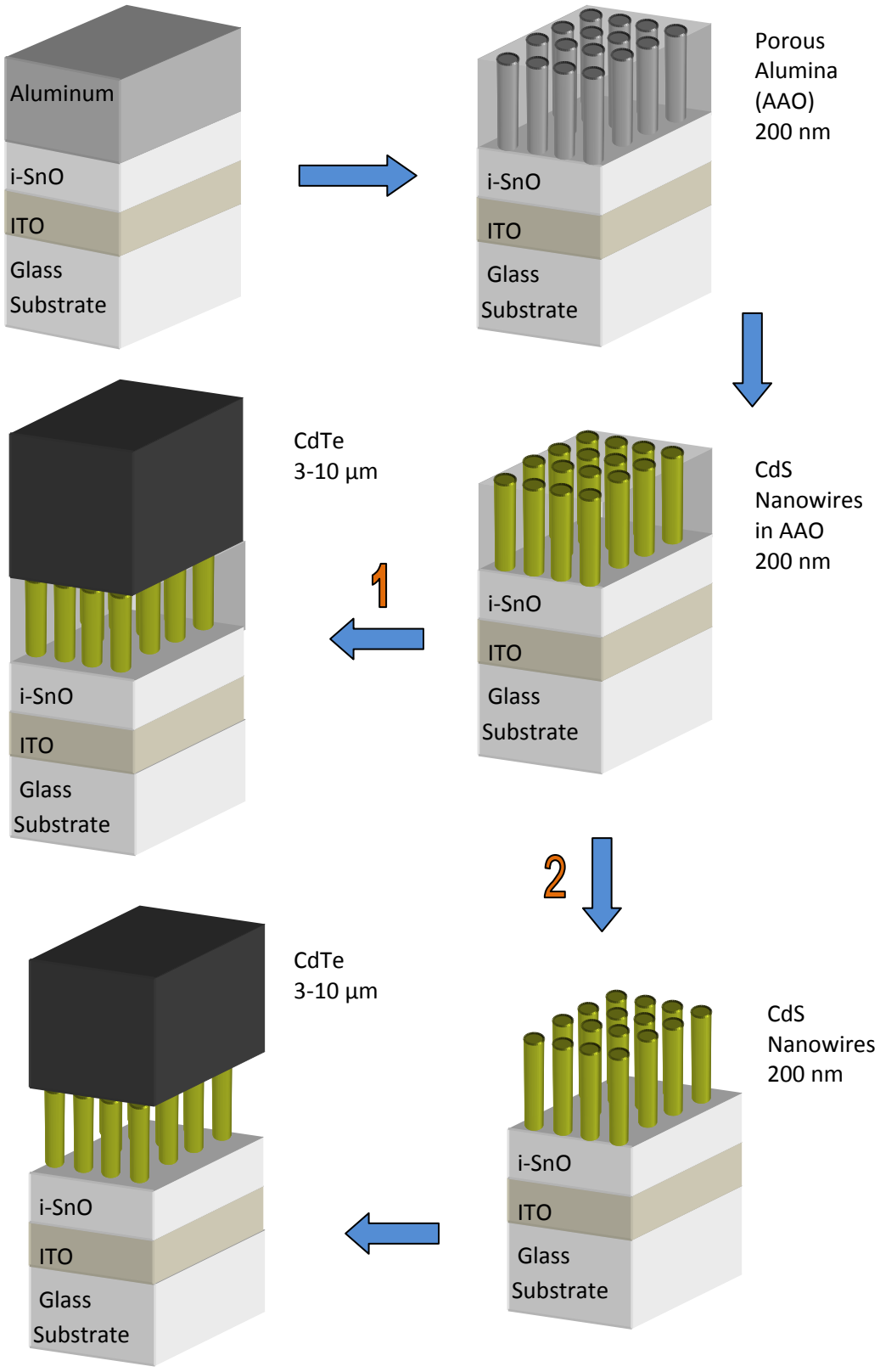

Figure 4.1 Flowchart of Fabrication of Nanowire CdS Solar Cells

4.1 Preparation of AAO Templates

An intrinsic tin oxide layer was deposited on ITO by sputtering as mentioned in previous chapters. Besides, another 5 - 10 nm thin titanium layer was deposited on top of i-SnO2 film directly through sputtering. It is used for enhancement of conductivity and adhesion for nanowires standing alone on substrates. Next, an aluminum layer with thickness of 100 to 250 nm was evaporated on top of the titanium layer by electron beam evaporation. Because next operation, anodization, may deplete a small portion of aluminum and hence 20 to 40 nm more aluminum was usually deposited.

The substrates were then anodized in oxalic acid. Solution for anodization can be 0.3 M oxalic acid or mixed acid of 14% H_2SO_4 and 4% oxalic. The oxalic acid used to make our devices is 0.3 M oxalic and kept in a temperature of 5˚C. Under constant voltage of 50 V and current of 0.1 A, substrates were charged as anode and platinum metal sheet was connected as cathode, to form anodized aluminum oxide (AAO) templates. Note that, titanium thickness will significantly affect the growth of AAO templates, either oxidation of titanium or thicker film will result in failure of AAO formation. Once AAO templates were formed, they were etched in 5% phosphoric acid at room temperature for 50mintures. After the phosphoric acid etching, Argon-based RIE (reactive ion etching) was performed to remove alumina barrier layer within AAO templates through plasma etcher. Etching rate depends on power, Argon flow rates, and chamber pressure and is controlled at 5nm/min. Some other groups[41] use a 20% HCl and 0.1 $mol \cdot L^{-1}$ $CuCl_2$ mixed solution as the after anodization etch solution and use 20% H_2SO_4 to dissolve the barrier layer.

4.2 DC Electro-deposition of CdS

The CdS wire arrays were grown in AAO templates by the electro-deposition process. The electrolyte for CdS nanowires deposition was a mixture of 0.5g cadmium chloride ($CdCl_2$) and 0.5g elemental sulfur in 50mL dimethyl sulfoxide (DMSO), with the formula of $(CH_3)_2SO$, solution. Concentrations are 0.055 $mol \cdot L^{-1}$ of $CdCl_2$ and 0.19

$mol \cdot L^{-1}$ of Sulfur in DMSO. Solution is heated to more than 100 ˚C and DC current is induced from anode platinum to AAO template cathode for the growing of the CdS wire arrays. An optimal electro-deposition condition was determined at current density of $7mA/cm^2$, and temperature 140 ˚C. The charged current and deposition time is impacted by the temperature of electrolyte, surface area squares, concentration of solution and distance between anode platinum and cathode substrates. After the electro-deposition, the AAO templates with CdS nanowires were immediately removed from the electrolyte. Firstly, substrates were rinsed with hot DMSO solution, and followed by acetone rinsing to remove organic adhesions on film surface. Then nanowire CdS film coated substrates were washed in DI water through sonication. After blown dry in nitrogen, substrates were ready for CdCl2 treatment and furnace annealing following the same process and conditions as what applied to planar CdS film fabrication, mentioned in previous chapter.

The AAO was then removed by dissolving the AAO templates in 1 M NaOH solution at room temperature for 50 minutes. And hence, CdS nanowires were directly mounted on substrates independently. To observe the characteristics of deposited CdS nanowire arrays, after annealing, substrates can be slightly etched in 1M NaOH solution for a few minutes only. Thus, only partial of wire arrays were exposed and can be used to form Schottky diodes, which is fabricated through deposition of a thin Au layer directly on CdS layer by thermal evaporation.

4.3 Other Procedures

Nanowire CdS solar cells shares the same procedures of making CdTe films and back contacts with CdS/CdTe solar cells with planar a CdS film. Also, nanowire CdS solar cells were measured by UV-absorption, four point probe Rs measurer, SEM, AFM, XRD and etc.

Chapter 5 Results and Discussions

Results of comparison between planar CdS films and nanowire CdS films through the characterization methods of light absorption, SEM images and XRD patterns are described in this chapter. Results from various related experiments and projects including the influence of CdS film thickness on solar cell performance, influence of NP etch, and Schottky diode characteristics, are also presented and analyzed.

5.1 Characterization from SEM Images

High density of CdS nanowires arrays were revealed in SEM (scanning electron microscope) images of top view and side view seen in Figures 5.1 and 5.2 respectively. These CdS nanowires have typical length of 100 nm and diameter of 40 nm and are vertically aligned on glass substrates. AAO templates have already been removed by dipping in NaOH solution and CdS nanowires are standing alone by themselves. CdS nanowires made from DC electro deposition method were very uniform and had high density. As estimated, more than 95% of nano-pores are filled with CdS nanowires, which grow all the way through the pores to the top surface of the glass-ITO-tin oxide substrate.

This well-aligned structure with vertical columns and rows is expected to lead to a larger current density, lower light absorption and consequently higher power conversion efficiency for the solar cells. The sunlight photons are completely locked in the nanowires with longer effective length through multiple reflections; also, space between CdS nanowires allows sunlight photons to pass through directly onto the CdTe film. Thus a substantially larger transmission of light can be expected and is indeed observed through UV absorption measurer.

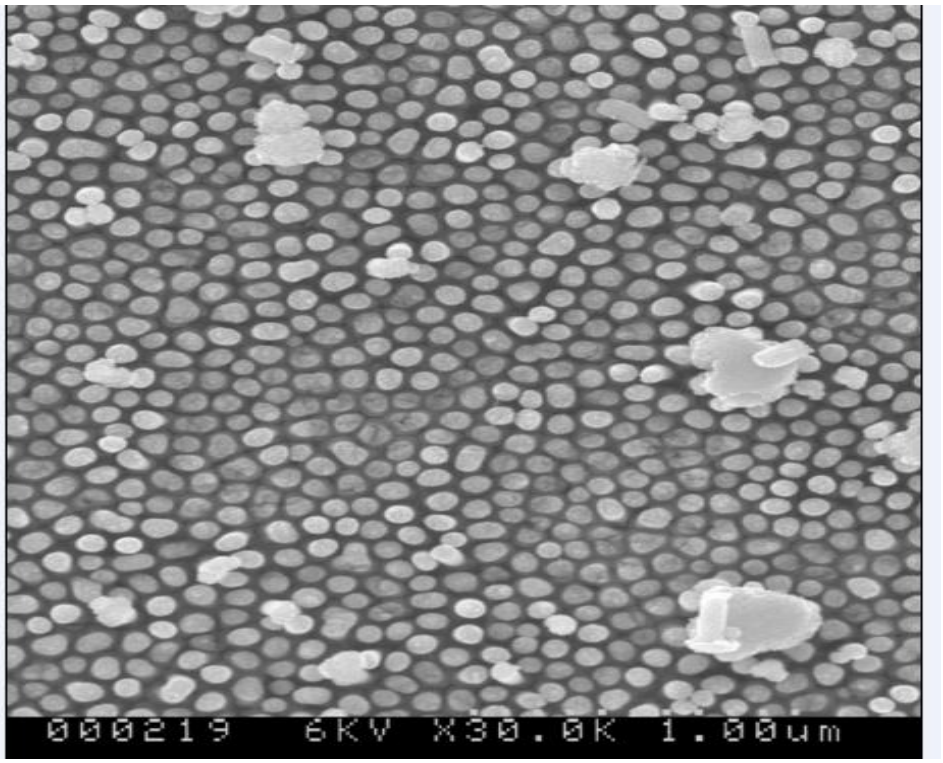

Figure 5.1 SEM Top View of CdS Nanowires

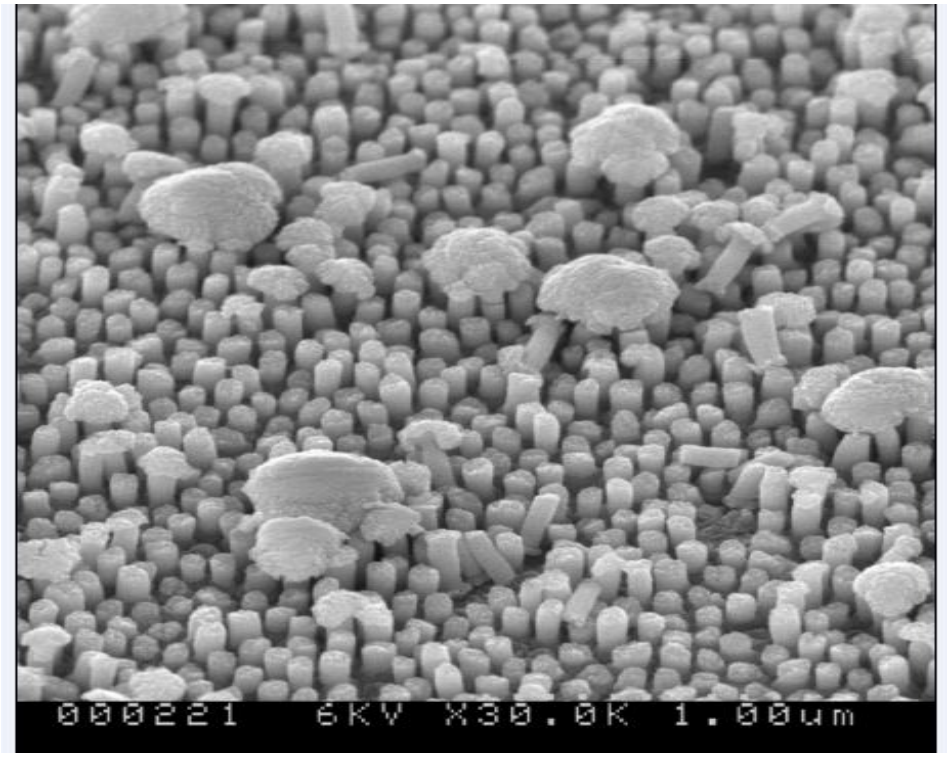

Figure 5.2 SEM Side View of CdS Nanowires

5.2 Characterization from UV Absorption

In CdS/CdTe solar cells, the energy transferred from sunlight to electricity is mostly from the part of light with wavelength between 300 nm to 800 nm, especially the blue light part locating in this range. Comparisons of absorption and transmission ability between CdS nanowires film and CdS planar film are shown in Figure 5.3 and Figure 5.4 respectively. This experimental data was obtained from a UV-absorption machine with substrates in a closed dark space and light of different wavelengths incident directly and normally onto the surface. The absorption in the glass-ITO substrate layer was experimentally subtracted by using that substrate layer as the "reference" or "background" layer for the absorption and transmission measurements.

In Figs 5.3 and 5.4, as expected, 100 nm thick nanowire CdS film shows the minimum absorbance when compared with the 200 nm thick nanowire CdS film and the 100 nm thick planar CdS film. In general, thinner films show lower absorbance because shorter transmission path reduces the probability of interaction between an incoming photon and the CdS film. Therefore, it is interesting to note that the thicker (200 nm) CdS nanowire film has lower absorption than the thinner (100 nm) planar CdS film. This is attributed to the facts that, (i) planar CdS film is solid while the nanowire CdS film has gaps between nanowires, which are totally transitive to the sunlight photons; (ii) effective energy bandgap of nanowire CdS film is higher than its planar CdS film counterpart because CdS nanowires are really stacks of very thin nano-discs, Thickness of these nanodiscs is less than the Bohr's radius for cadmium sulfide, which is estimated to be 4 nm. Thus CdS nanowires are able to exhibit quantum confinement effects, which result in higher energy band gap and substantially reduced absorption in the ultra-violet portion of the solar spectrum.

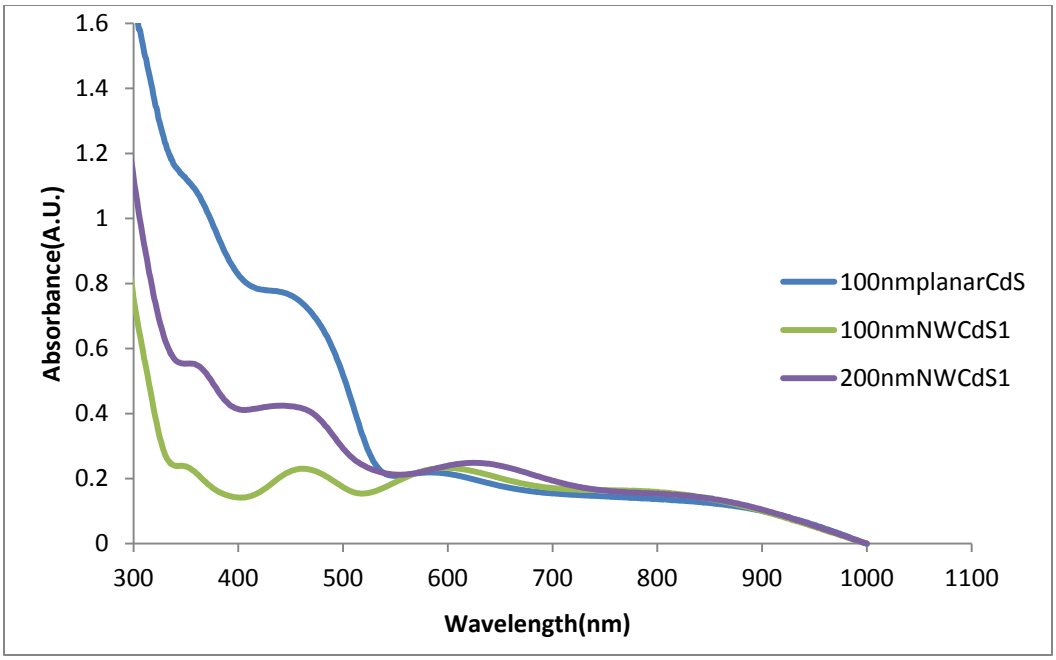

Figure 5.3 Comparison of absorbance

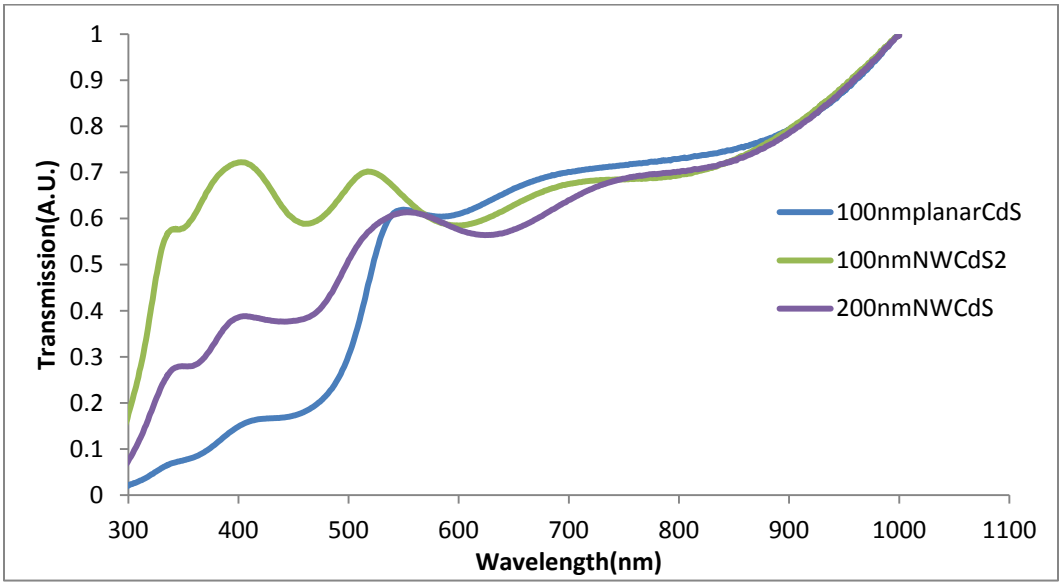

Figure 5.4 Comparison of transmission

5.3 Characterization from XRD Images

XRD (X-ray Diffraction) measurements collect data through an X-ray diffractometer using the Cu K_α radiation in the 2θ geometry; this is an extensively used technique for characterizing atomic-scale structures. Figure 5.5 - 5.7 present XRD patterns of CdS films fabricated in different structures, of 100 nm planar film, 200 nm nanowires and 100 nm nanowires respectively in AAO templates.

All films were found to be of hexagonal lattice structures. In all three XRD images, there is a peak for the (002) plane which responds to the hexagonal CdS. Small diffraction peaks were found in (101) and (103) planes. And the intensities of these two planes in nanowire CdS films are much less than the intensity of (002) plane, which suggested the growth of CdS nanowire were along the c-axis orientation. Planar CdS film, with more than one X-ray diffraction peaks, was grown and spreading in more than one direction, while the XRD patterns indicates that the nanowire arrays are mainly oriented in (002) plane, a preferred c-axis direction. Meanwhile, the intensity peak of planar CdS film (less than 120) was smaller than that of nanowire CdS films (between 120 to 140). Additionally, thinner nanowire CdS films had better growth in the AAO membranes; this is reflected by the larger intensity and fewer additional X-ray diffraction peaks. Overall, the qualities of CdS films revealed by XRD analysis showed an improvement by applying nano-structures and reducing the length of nanowires (see figure 7).

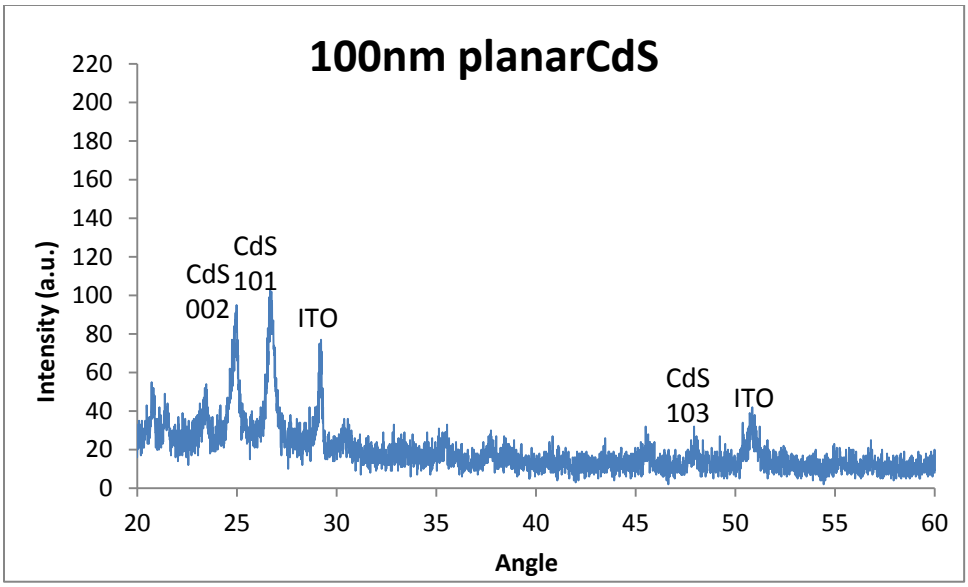

Figure 5.5 XRD Image of 100 nm Planar CdS film

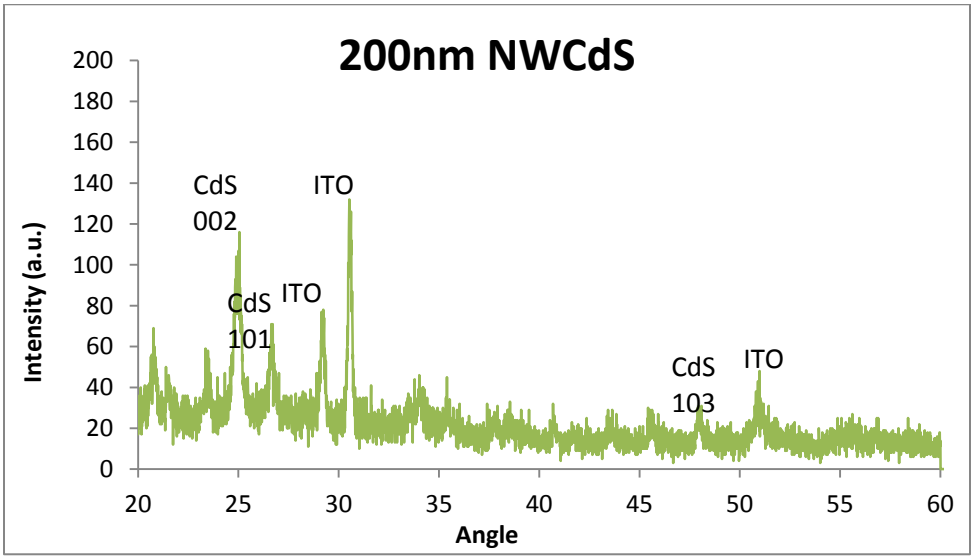

Figure 5.6 XRD Image of 200 nm Nanowire CdS film

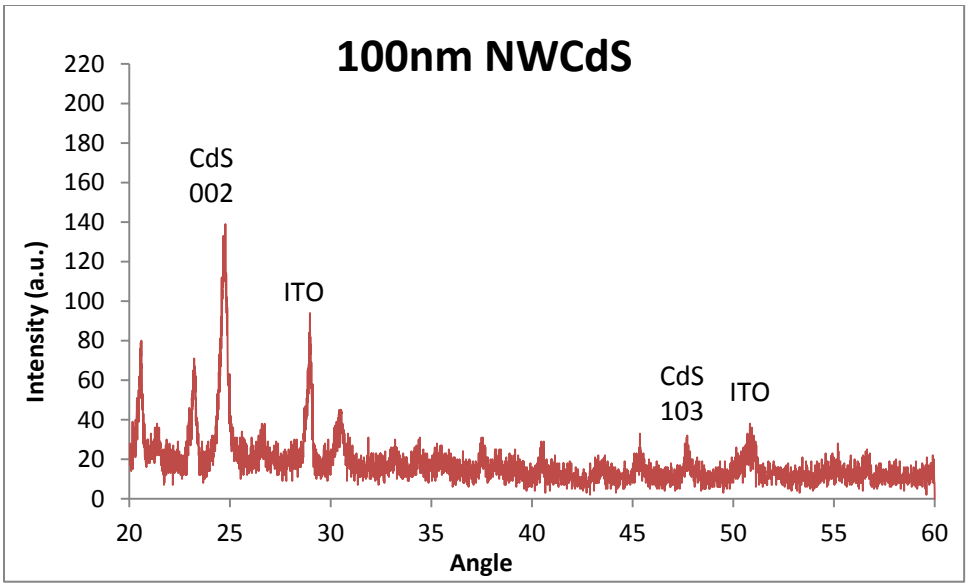

Fig. 5.7 XRD Image of 100 nm Nanowire CdS film

5.4 Comparative Analysis of CdS Films Fabricated from Different Solutions and Methods

5.4.1 Optical Transmission

CdS-CdTe solar cells with CdS films made from thermal evaporation were prepared and their characteristics compared with the characteristics of solar cells using the CdS films made by the method of chemical bath deposition (CBD). Also, CdS layers made by CBD from titration of different solutions and different times of dips were prepared and used for making CdS-CdTe solar cells for comparative evaluation. Figure 5.8 illustrates the absorption of substrates with CdS made from different procedures. Table 5.1 lists the concentration values of different solutions used for CdS deposition.

Based on the data from the curves of Figure 5.8 and Table 5.1, the substrate L3-4 has 3 dips of CdS from solution 1 and thus has the largest thickness, which results in its transmission being the minimum among all samples. The samples L3-1 which was made from Solution 3 has the largest transmission because solution 3 has lowest concentration and it was made through titration. The transmission of sample L3-2 made from solution 2

has the second largest value since solution 2 has second lowest concentration and this sample was also made through titration. Also, as the number of dips while making the CdS film was increased, the transmission decreased, as one might expect from the increased thickness of film. In summary, absorption decreased with increase in solution concentration and the number of dips.

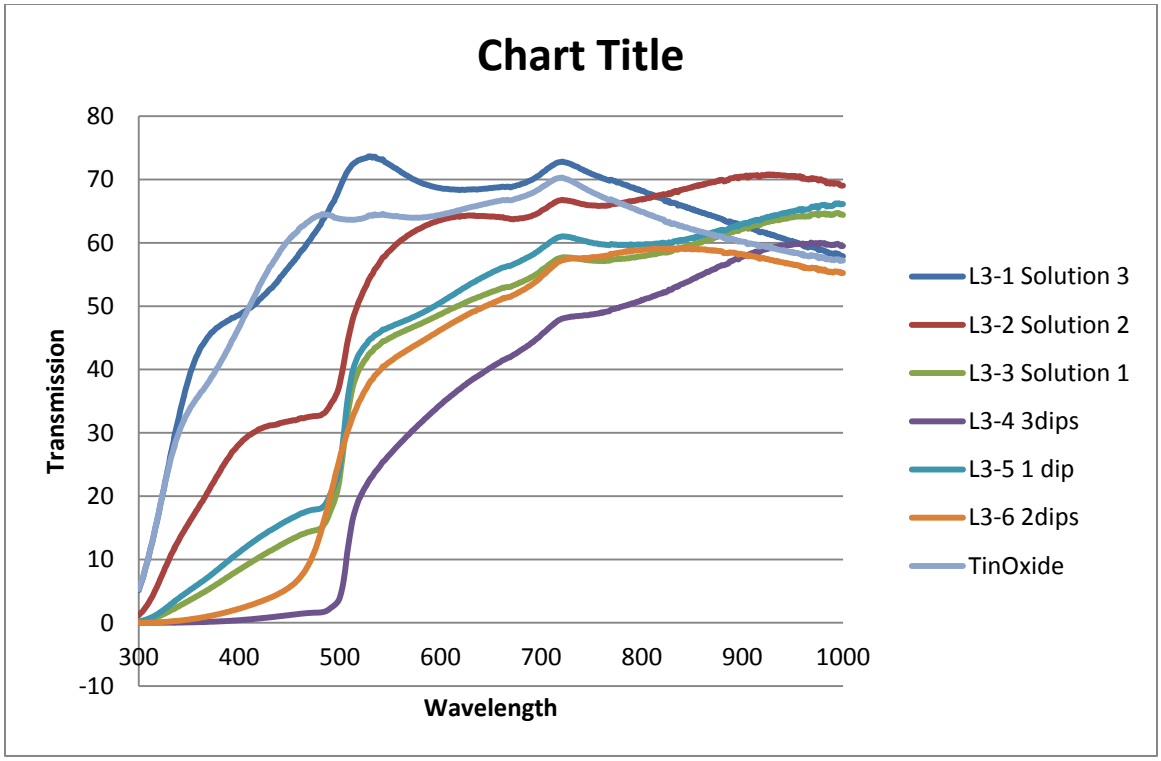

Figure 5.8 Transmission of L3 series substrates

Table 5.1 Concentration of Components of 3 CdS Solutions

Chemicals	Solution 1 0.15M	Solution 2 0.05M	Solution 3 0.012M
NH4OH (ml)	5.4	4	5.45
CdCl2 (g)	0.73	0.368	0.30
NH4Cl (g)	0.72	0.268	2.675
Thiourea (g)	2.3	0.76	0.255
Time (Minutes)	8	10-15	38
Temperature (Degree C)	80	70(88)	88

5.4.2 Open Circuit Voltage of CdS-CdTe Junction

Using $CdCl_2$ treatment and CSS process, several micrometers of bulk polycrystalline CdTe films were deposited on top of CdS substrates prepared under the conditions described above in Section 4.2. Once CdTe was coated, values of open circuit voltage (Voc) were measured after every subsequent step taken. Measured Voc values are shown in Table 5.2 for eight experimental devices whose details are as follows: CdS films of sample 1, 2 and 8 were made through solution 1 respectively by 3 dips, 2 dips and 1 dip, CdS films of sample 3, 5 and 6 were made respectively from solution 1, 2 and 3 whose component concentrations were illustrated in Table 5.1, and sample 4 had its CdS made from solution 1 and first layer of CdTe made from ED method. In this Table, the NP etch time is determined basing on the generation of bubbles and covering the whole CdTe film. The lowest Voc value comes from samples made by solution 3 and best Voc results from Solution 1. This fact indicates that adding components by titration is a better method then through whole dip. We believe that through titration, fabricated CdS films are more uniform and have less pin holes which may largely impede the device performance.

Table 5.2 Voc of Sample Devices after Every Procedure

Sample Order	Solution /Method	Voc after CdTe Deposition (mv)	Voc After annealing(mv)	NP etch time(s)	Voc After NP etch(mv)
1	3 dips	412	548	23	588
2	2 dips	384	487	22	524
3	Solution #1	399	520	20	601
4	CdS/CdTe/CdTe 1	416	475	28	510
5	Solution #2	249	484	24	431
6	Solution #3	346	394	21	360
7	CdS/CdTe/CdTe 2	314	440	24	572
8	1 Dip	325	480	20	500

Observing the Voc data of samples made from different number of CdS dips, the more dips taken, the higher Voc is achieved. This phenomenon can be explained by following reasons:

1.CdS is consumed or sublimated during CSS process, and the samples from 3 dips has the thickest CdS film which enables the creation of better junction;

2. CdS thickness of 3 dips samples is closer to the theoretically ideal thickness;

3. CdS films of 3 dips samples have least pin holes because CdS was deposited layer by layer and pinholes were covered by later layers.

Basing on experiments, CdS sublimation is possible when CSS temperature is as high as 675 ˚C. Many samples were damaged in our pursuit of higher CSS temperature for making higher quality junctions. Pin holes on CdS film are very difficult to observe. However, after the deposition of CdTe, pin holes become clearly identifiable. The third reason proposed above is confirmed by experiments that showed that more pin holes were present on sample devices which had thinner CdS films and no pin hole were visible on device made from 3 dips of CdS.

To test and verify the second reason and find out the value of CdS thickness for the highest efficiency, another project was undertaken where, in order to make CdS films with accurate thickness, the technique of thermal evaporation was applied. Results of that project are described later in next section below. But before that, more results can be presented from this project. Table 5.3 below lists Voc values of experimental solar cell devices after the deposition of top contact dots, which are made by coatings of thin copper, graphite and silver respectively annealed in Nitrogen.

Table 5.3 Voc of Contact Dots of Sample Devices

Solution /Method	Contact Dot 1	Contact Dot 2	Contact Dot 3	Contact Dot 4	Contact Dot 5	Contact Dot 6
solution #1	614	621	604	617	603	601
Dip 1	428	446	357	242	285	161
Solution #2	236	236	163	210	246	351
Solution #3	138	161	N/A	N/A	N/A	N/A
Dip 2	508	500	494	499	494	485
Dip 3	544	531	561	563	525	512
CdS/CdTe/CdTe 1	410	289	325	276	119	37
CdS/CdTe/CdTe 2	473	467	462	455	470	427

Unfortunately, the film made from solution 3 is too thin to survive from CSS and NP etch procedures. The left part of film was only sufficient for making two contact dots. Furthermore, the observed open circuit voltage was very low. Samples made from solution 2 also exhibited low Voc. These data confirm excessively thin CdS would lead to poor cell performance, which is in conformity with the data from Table 5.2. Devices made from titration of Solution 1 yield not only the highest Voc values but also display uniformity; open circuit voltages of different contact dots are so close that it means that the CdS and CdTe films deposited are very uniform.

It is interesting to note the results from the experimental devices CdS/CdTe/CdTe 1 and CdS/CdTe/CdTe 2, which are made with layers of CdS from CBD, CdTe from electro-deposition (ED) followed by CdTe from CSS. These two series of sample are multi-junctions CdS-CdTe solar cells, which our group is the first one to experiment with. We were fortunate to observe some good values from these samples even though the device performance is not sufficient to justify changes in manufacturing processes.. Still, the open circuit voltage values of multi junction devices are promising to compete with single junction devices. In Table 5.2, the values of voltage are not much behind. In

addition, in Table 5.3, uniform values were found in Series 2 of CdS/CdTe/CdTe samples.

5.5 CdS Films of Different Thicknesses Deposited by Vacuum Evaporation

In experiments described above in Section 5.4, the open circuit voltages of CdS-CdTe solar cells were found to increase along the increase of thickness of the CdS layer. To find out the best value of CdS thickness for fabricating planar CdS/CdTe solar cells, a project to fabricate accurate thickness of CdS films by vacuum evaporation was undertaken. CdS films were deposited by thermal evaporation with defined thickness between 50 to 1000 nm. Also, CdS substrates made from CBD were prepared for comparison. To make CdS layers with different thicknesses by CBD, samples were made with different number of dips. The thicknesses picked to conduct experiments included 100 nm, 150 nm, 200 nm, 400 nm and 1000 nm. To find out which method is more advantageous in forming CdS films, several series of sample devices made by CBD titration were prepared. The CdS films made from one titration samples have thickness about 100 nm and CdS films made from 2 times of titrations have thickness between 150 nm to 200 nm.

Table 5.4 includes all detailed data about the methods of CdS films made, the CdTe taken environmental condition, CdTe thickness, open voltages before $CdCl_2$ treatment and even the CSS experiments conducting round sequence.

The sample devices with very thick CdS films, 400 nm or 1000 nm, are not able to survive even in other procedures. The films are so thick that during $CdCl_2$ treatment step the growths of crystal grains break the structure of films and result in its being unable to stick to glass substrates during later process steps, especially in the NP etch step. Thus, no data was captured for overly-thick CdS films and compared thicknesses with valuable data include only 100 nm, 150 nm and 200 nm. All sample devices are sorted by the method of CdS film deposition and thickness.

To analyze the devices from CBD only, 2 titrations method fabricates much better CdS films, with Voc values about 20% higher than those from 1 titration method. Possible reasons have been explained in Chapter 5.4, and the reduction of pin holes is a big contribution to the voltage improvement through visible observation.

Basing on the voltages obtained from the thermal evaporated made devices, 150 nm CdS device and 200 nm CdS device possess much higher Voc than that of 100 nm CdS device. The highest value is found in 200 nm CdS device, but not larger enough than the highest voltage of 150 nm CdS device. Voltage data has been selected in the Figure below (Figure 5.9). Basing on the curves, there is not much difference between these two series of devices.

Table 5.4 Data of Project HEP 4

Sample Order	CdS method	CdS Thickness (nm)/CBD titration times	Voc (mv)	CdTe Thickness (um)	CSS Condition	Voc after CdCl2 Treatment & Annealing
1	CBD	1 time	370, 424 451, 433, 417	3	550/625 ˚C 30S 2m45s 10t H	346, 310 343 344, 329
2	CBD	1 time	N/A	4.5~5	550/625 ˚C 30s 2m41s 10t H	539, 583 414 500, 497
3	CBD	2 times	421, 311 359, 388, 327	11	525/625 ˚C 90s 1.14t A	579, 603 595 628, 625
4	CBD	2 times	363, 383 373, 355, 335	10	525/625 ˚C 90s 1.14t A	654, 589 625 631, 579
5	TE	100	469, 519 583, 446, 511	3	550/625 ˚C 30S 2m45s 10t H	299, 366 438 404, 379
6	TE	100	N/A	4.5~5	550/625 ˚C 30s 2m41s 10t H	390, 381 311 316, 204
7	TE	150	373, 290 270, 383, 307	2.5~3.5	525/625 ˚C 60s 1.14t A	631, 639 565 620, 600
8	TE	150	376, 359 394, 371, 415	2.2~3	525/625 ˚C 20s 1.14t A	567, 567 574 566, 544
9	TE	200	333, 431 344, 359, 379	3~3.5	525/625 ˚C 20s 1.14t A	610, 580 593 597, 588
10	TE	200	428, 298 380, 406, 334	3.1~4.1	525/625 ˚C 60s 1.14t A	627, 645 630 620, 654
11	TE	400	N/A	N/A	N/A	N/A
12	TE	1000	N/A	N/A	N/A	N/A

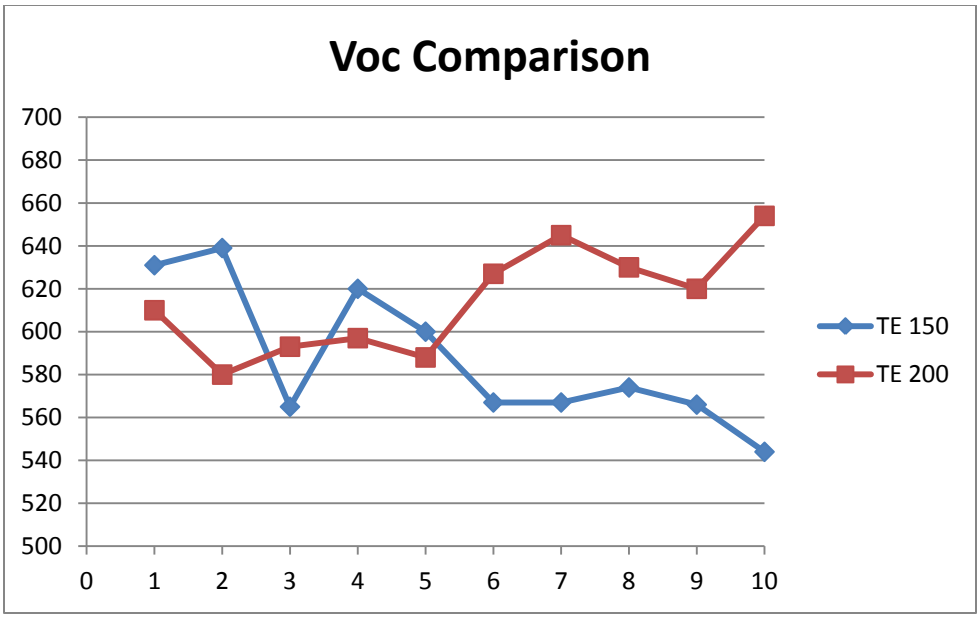

Figure 5.9 Open Circuit Voltages of Thermal Evaporation Made Devices

The ideal thickness of CdS film is about 80 nm to 100 nm, which is used by many professional labs. However, the best thickness matching the lab condition should be picked. In our lab, it is between 150 nm and 200 nm. To explain the mechanism that causes the difference, we proposed a hypothesis is proposed, the CSS system consumes part of CdS before the sublimation of CdTe, which has been verified by our experiments. In the CSS process, the normal setting of temperature is to preheat both substrates and source temperature to 350 ˚C, input helium, wait pressure to stabilize, and then increase temperature directly to 525/625 ˚C (525 is the substrate temperature and 625 is the CdTe source temperature). As we know, the CdTe starts to sublimate at a temperature of 460 ˚C. When substrates are preheat to 450 ˚C and sublimation temperature is set as 580/625 ˚C or higher, CdTe cannot be deposited on substrates and most of CdS films are gone. To avoid the disappear of CdS and keep substrate temperature at a value higher than 525 ˚C, substrate and source temperatures are both kept in the same pace increasing from 300 to 550, and then heat the source temperature to 625 ˚C and kept for a specified duration. Through this, good devices with CdTe coated on CdS films are fabricated. However, the CdS sublimation is not completely eliminated. Still, CdS was found disappear in sample substrates. Considering the fact that CSS system consumes part of CdS films, thicker CdS

films are needed for the use in out lab. And the best matching value is between 150 nm and 200 nm.

Some labs are using CSS system to form CdS films on glass substrates and the temperature used is about 475 ˚C[42]. It means that in the CdTe deposition process by CSS, the possibility of CdS sublimation exists by any means. However, good CdS/CdTe junctions can only be made during high temperature which is much larger than 475 ˚C. CdS sublimation largely impacts the power conversion efficiency through introduced impurities and thinner the junction. Also, once the CSS system, especially the graphite made substrate holder is contaminated, every experiment conducted afterwards will not be perfect. The quartz tube of the CSS system is easy to clean by using nitric acid and organic cleaning liquids. But the substrate holder is very difficult to clean and it can only be replaced. Therefore, the CdS contamination should be avoided to the largest extent. Ways to mitigate the CdS sublimation includes, upgrading the CSS heating components to shorten the temperature increase time to the minimum, upgrading the gas pump to ensure the vacuum environment, and upgrading the power controllers to improve the efficiency of temperature adjustment.

5.6 Current-Voltage Characteristics

Well fabricated devices are placed on top of AM1.5 sunlight simulator system and voltage and current data are collected through a programmable power generator system and Lab View programmed software package. Data is analyzed by MATLAB coded program and I-V curves generated automatically. I-V curves can be converted into J-V curves by adding the factor of contact area. From the I-V curves include curves in dark condition and curves in light condition. Information of diode properties can be read from dark conditional curves and data of efficiency, fill factor, resistance, open circuit voltage and short circuit current can be determined from light conditional curves. Figure 5.10 is a classic I-V of completed sample device.

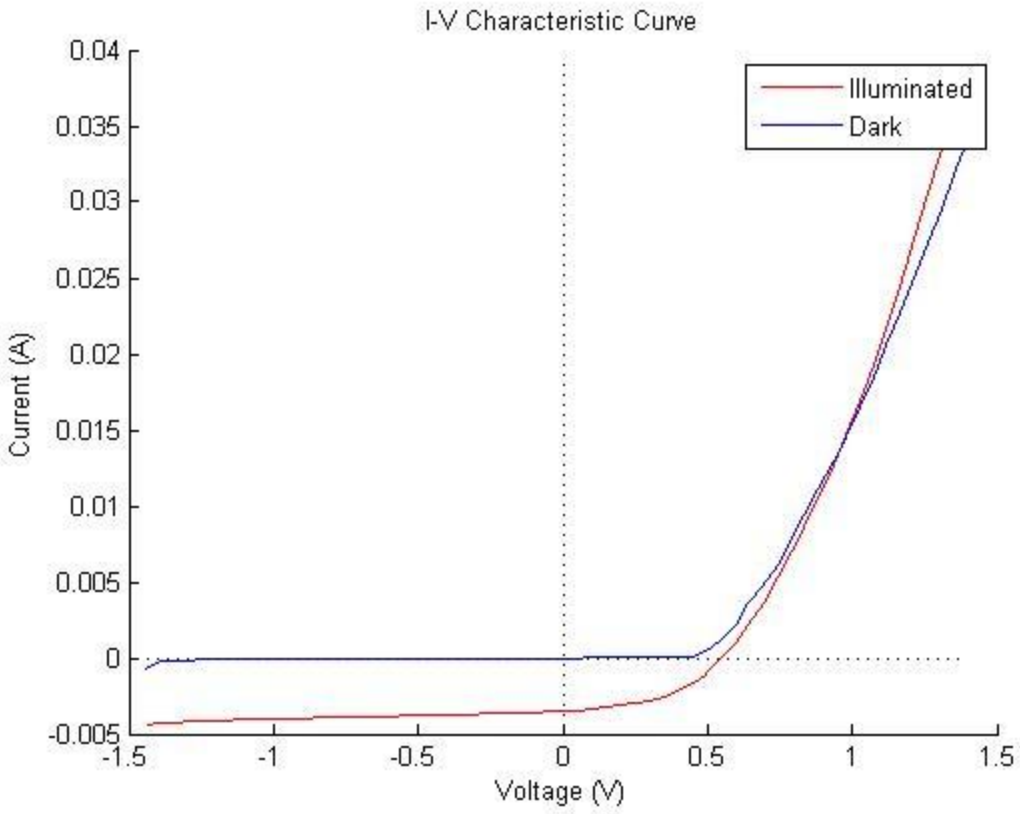

Figure 5.10 I-V Curve of A TE 150 nm CdS/CdTe Solar Cell

The red curve is the captured under illuminated and the blue curve is captured in dark condition. Open circuit voltage is read when current is zero and short circuit current is obtained when voltage is zero. The power fill factor is determined as the equation (Equation 5-1) below.

$$FF = \frac{P_{max}}{V_{oc} \times I_{sc}} \qquad 5\text{-}1$$

P_{max} is determined basing on the red curve by picking the maximum multiplicative value of voltage and current. In ideal condition, the red curve should be shifted towards the positive side. However, due to the existence of sheet resistance, which consumes electric energy that converted from solar power, the real electric power generated is smaller than the power converted by the solar cell. Assuming P_{conv} is the energy converted from

sunlight, I_{max} is the current when P_{max} is achieved and R_s is the value of sheet resistance, the mechanism can be explained by the Equation 5-2.

$$P_{conv} = P_{max} + I_{max}^2 \times R_s \qquad 5\text{-}2$$

On the other hand, the real open circuit is also mitigated due to sheet resistance. Therefore, it is significant to reduce the value of the sheet resistance to its minimum. This factor has been considered since the step of choosing good ITO glass substrates.

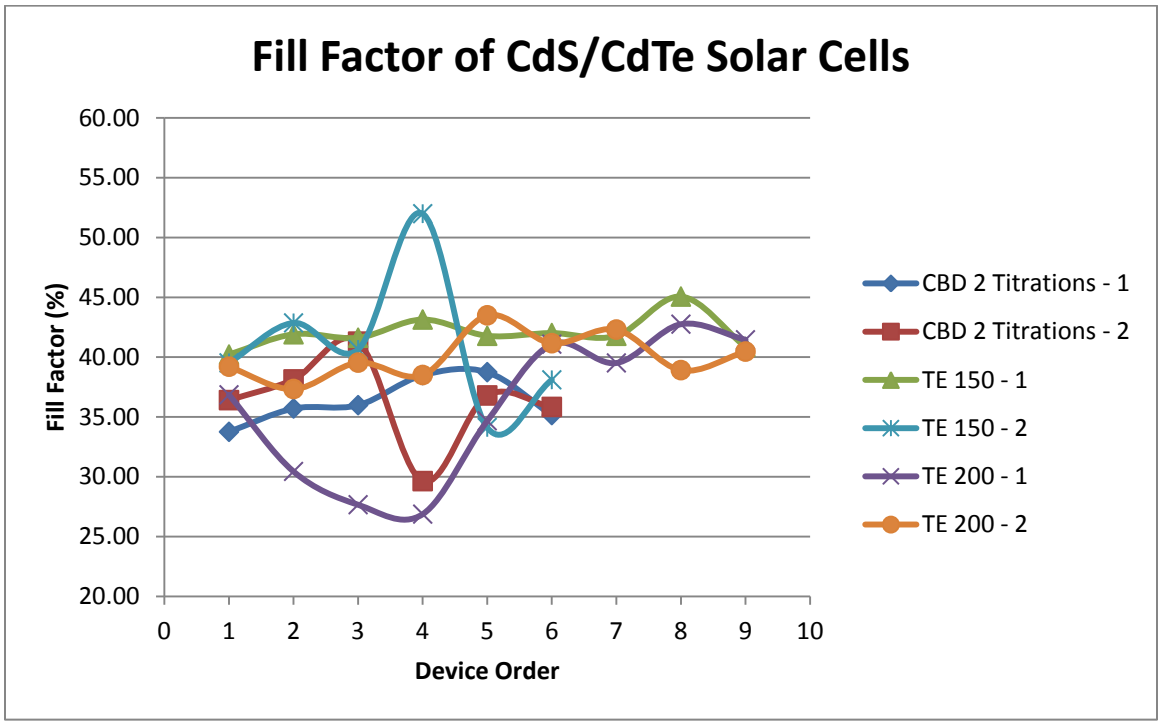

Figure 5.11 Fill Factors of CdS/CdTe Solar Cells

Fill Factors of sample devices made in HEP4 (High Efficiency Project #4) are shown in Figure 5.11 above. Only sample devices with Voc larger than 500 mV are selected. From the 6 curves, TE 150 devices possess larger and more balanced scattered fill factors. TE 200 devices has 200 nm CdS films, which is 50 nm thicker than TE 150 devices, and hence the averaged sheet resistance is larger than that of TE 150 devices.

The increased sheet resistance occupies more voltage as Equation 5-2 explained when converting energy. This is confirmed by Figure 5.12 as below.

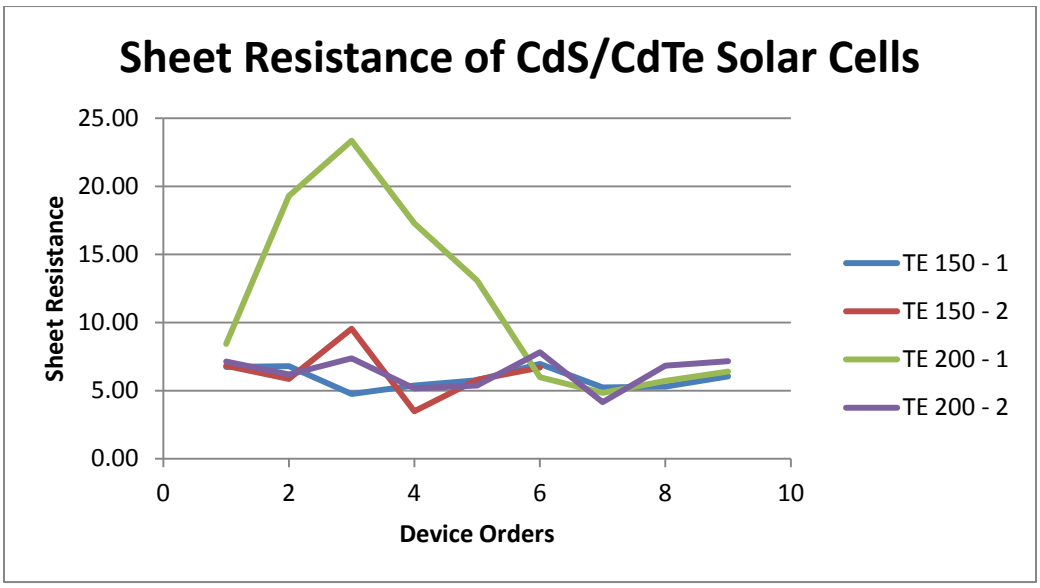

Figure 5.12 Sheet Resistance of CdS/CdTe Solar Cells

The average value of sheet resistance of the TE 200 series is 8.98 comparing 6.08 of TE 150 series. To select the best thickness for CdS samples, both Voc and fill factor should be considered. Based on current experiment data, devices of 150 nm thickness will be better since the difference between TE 150 and TE 200 not large enough to cover the disadvantages caused by sheet resistance. However, more lab work should be done and devices with higher Voc and fill factors should be fabricated to confirm this result.

Chapter 6 Conclusions and discussions of current limitations and scope of the future work

CdS/CdTe solar cells with planar CdS films and cells with nano-wire CdS are fabricated. Their properties are characterized and analyzed based on experiments and semiconductor theories. The application and fabrication processes of CdS/CdTe solar cells with planar CdS films are introduced and many projects are conducted in order to figure out the ideal condition to reach the best power conversion efficiency. Procedures to fabricate traditional CdS/CdTe solar cells are presented in detail, as well as the procedures to fabricate nanowire CdS films. Theoretically, the nanowire CdS has better light transmitting property; this was later confirmed by experiments through applications of UV-absorption, XRD and SEM images. Also, its potential enhancement to solar cell efficiency was introduced in theory. Several projects about key factors influencing solar cell efficiency were discussed. Different methods of CdS deposition were mentioned and the best thickness of CdS films in EDRL environment was found to be 150 nm, based on the analysis of the open circuit voltage, fill factor, light absorption and sheet resistance.

However, the open circuit voltages of fabricated devices are limited by many conditions and not sufficient to build a high efficiency module. One restriction that impedes obtaining high efficiency is the CSS system used in EDRL. The heating process costs too much time which results in difficulty of determining right sublimation time. In addition, the heating lamps were not installed in balance and hence even two samples made from one CSS round own different CdTe thickness. And the consumption of CdS makes the inside CSS environment contaminated and causes a serious problem in making good junction, which is the key factor in fabricating a successful solar cell. While presently the best CdS/CdTe solar cells are all fabricated through CSS system, thermal evaporation or sputtering machine can be used to deposit CdTe films to avoid above problems. Other related properties can be observed and discussed and influence by equipment limitations can be eliminated.

Another way to improve the device performance is to inlet Hydrogen into CSS process rather than Helium or Argon. Some groups have found the improvement of using Hydrogen. But the real mechanism remains unknown.

Even though experimental experiences and most publications show that CdS films made from CBD method are more efficient, to fabricate better planar CdS films, other thin film deposition options should also be attempted, including thermal evaporation, sputtering machine and CSS system. Through thermal evaporation and sputtering machine, CdS films are more uniform and can be made with accurate thickness.

The nanowire CdS techniques are under development. Its valuable potential has attracted a lot of attention. The highest efficiency of nano-structural CdS/CdTe was fabricated in EDRL with 6.5% [21]. Also, nano-structural devices with higher efficiency are in processing. The nano scale devices are brand new to most groups and many creative structures are available for observation, such as CdS nano-tubes, CdS nano particles on CdS planar films, CdTe nanowires, CdS/CdTe/CdTe multi-junction, and etc.

To enhance the performance of ITO layer in the device, the fabrication of Tin Oxide is observed. Through annealing in nitrogen before CdS deposition, the improvement of light transmission was observed, but it increases sheet resistance a lot. In addition, other materials can be used to make transparent conductive oxide (TCO) layer. Some promising materials have been proposed by NREL and other groups.

Also, the methods of forming contacts should be upgraded. Besides copper, some other materials are in research in EDRL. The thickness, components of materials, fabrication environments are all under experiments. Materials like ZnTe, Sb2Te3, NiTe2 and molybdenum are good options.

At last, the $CdCl_2$ treatment presents remarkable improvement in strengthening the device performance. However, the treatment method of most groups is to leave samples in inert gas for annealing. The mechanism of $CdCl_2$ vapor on the growth of CdS crystals and CdTe crystals are not well analyzed. The chemical equation of reaction is known while the ideal temperature, pressure and amount of $CdCl_2$ vapor are unknown.

Projects should be conducted to observe the effects of over annealing on device performance. A face-to-face annealing project was conducted in EDRL of which the results showed that Voc were improved. However, as the CdTe crystals grows too large that CdTe films were not stable and fell off during NP etch process. Considering this failure, a new project about face-to-face annealing and NP etch should be done to reach a balance between high open circuit voltage and good film quality.

Appendix I MATLAB Codes

MATLAB codes to determining I-V curves and other solar cell factors

```
clear all; clc;
close all;
format long;

% Set variables
contactarea = 0.07/10000;       % contact area in meters
cdteeps = 10.6;
eps0 = 8.854e-12;               % in meters

% Load and sort light curve data
lightfile = 'Sample 13\13-21L.xls';         % input light excel sheet
file
 darkfile = 'Sample 13\13-21D.xls';         % input dark excel sheet
file
ldata = load(lightfile);
lvoltage = ldata(:,2);
lcurrent = ldata(:,3);
lcurrdensity = ldata(:,5)*0.07;

% Load and sort dark curve data

ddata = load(darkfile);
dvoltage = ddata(:,2);
dcurrent = ddata(:,3);
dcurrdensity = ddata(:,5);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Light curve analysis
[currmin, iidx] = min(abs(lcurrent));
[voltmin, vidx] = min(abs(lvoltage));

isc = lcurrent(vidx);           % Short-circuit current
jsc = lcurrdensity(vidx);       % Short-circuit current density
voc = lvoltage(iidx);           % Open-circuit voltage

p = zeros(iidx - vidx + 1,1);
for i = 1:length(p)
    p(i) = lvoltage(i+vidx-1)*abs(lcurrent(i+vidx-1));
end

[pmax, pidx] = max(p);
vmax = lvoltage(pidx + vidx - 1);
imax = lcurrent(pidx + vidx - 1);
jmax = lcurrdensity(pidx + vidx - 1);

ff = (vmax*imax)/(isc*voc);             % Fill factor
eta = (vmax*abs(imax))/(1000*contactarea);      % Efficiency
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Corrected for Series Resistance

% Series resistance
RserL = (lvoltage(iidx+1)-lvoltage(iidx-1))/(lcurrdensity(iidx+1)-...
    lcurrdensity(iidx-1));

correctedlvoltage = lvoltage - lcurrdensity*RserL;        % Vtrue = V -
IRs
Rserp = zeros(iidx - vidx + 1,1);
for i = 1:length(Rserp)
    Rserp(i) = correctedlvoltage(i+vidx-1)*abs(lcurrent(i+vidx-1));
end

[Rserpmax, Rserpidx] = max(Rserp);
Rservmax = correctedlvoltage(Rserpidx + vidx - 1);
Rserimax = lcurrent(Rserpidx + vidx - 1);
Rserjmax = lcurrdensity(Rserpidx + vidx - 1);

Rserff = (Rservmax*Rserimax)/(isc*voc);
Rsereta = (Rservmax*abs(Rserimax))/(1000*contactarea);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Plots

% Light and dark I-V curves
figure(1)
plot(lvoltage,lcurrdensity,'r-',dvoltage,dcurrdensity,'b-');
 plot(correctedlvoltage,lcurrdensity,'r-');
legend('Illuminated','Dark');
title('J-V Characteristic Curve');
box off; hold on
plot([min(lvoltage) max(lvoltage)],[0 0],'k:');
plot([0 0],[min(lcurrdensity) max(lcurrdensity)],'k:');

figure(2)
plot(lvoltage,lcurrent,'r-',dvoltage,dcurrent,'b-');
legend('Illuminated','Dark');
title('I-V Characteristic Curve');
box off; hold on
plot([min(lvoltage) max(lvoltage)],[0 0],'k:');
plot([0 0],[min(lcurrent) max(lcurrent)],'k:');
```

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